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Continuous-Time CMOS Quantizer For Ultra-Wideband Applications

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Outline

1. Introduction

2. The proposed quantizer description

- **Amplifier stages**
- **Threshold circuit**

3. Simulated results

4. Conclusions

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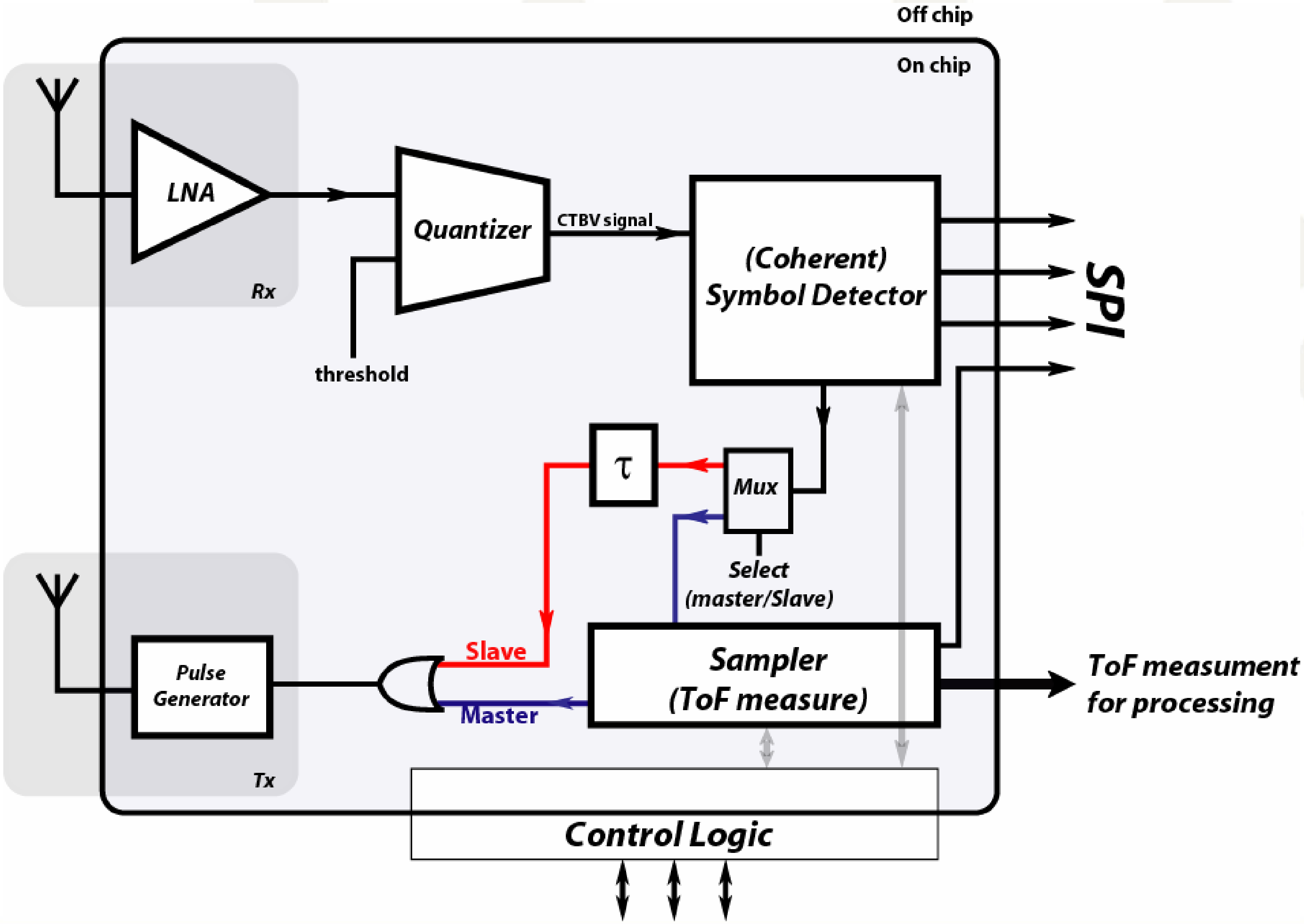
Introduction (1)

The 1st version of the active echo



Introduction (2)

• Proposing a solution for continuous-time, high-gain quantizer suitable for ultra wideband applications.

• A bandwidth exceeding 10 GHz is feasible while maintaining sufficient DC gain for the thresholding operation.

• The proposed solution is designed in 90nm TSMC technology exploring resistive-feedback inverters and a single LC resonator at the input.

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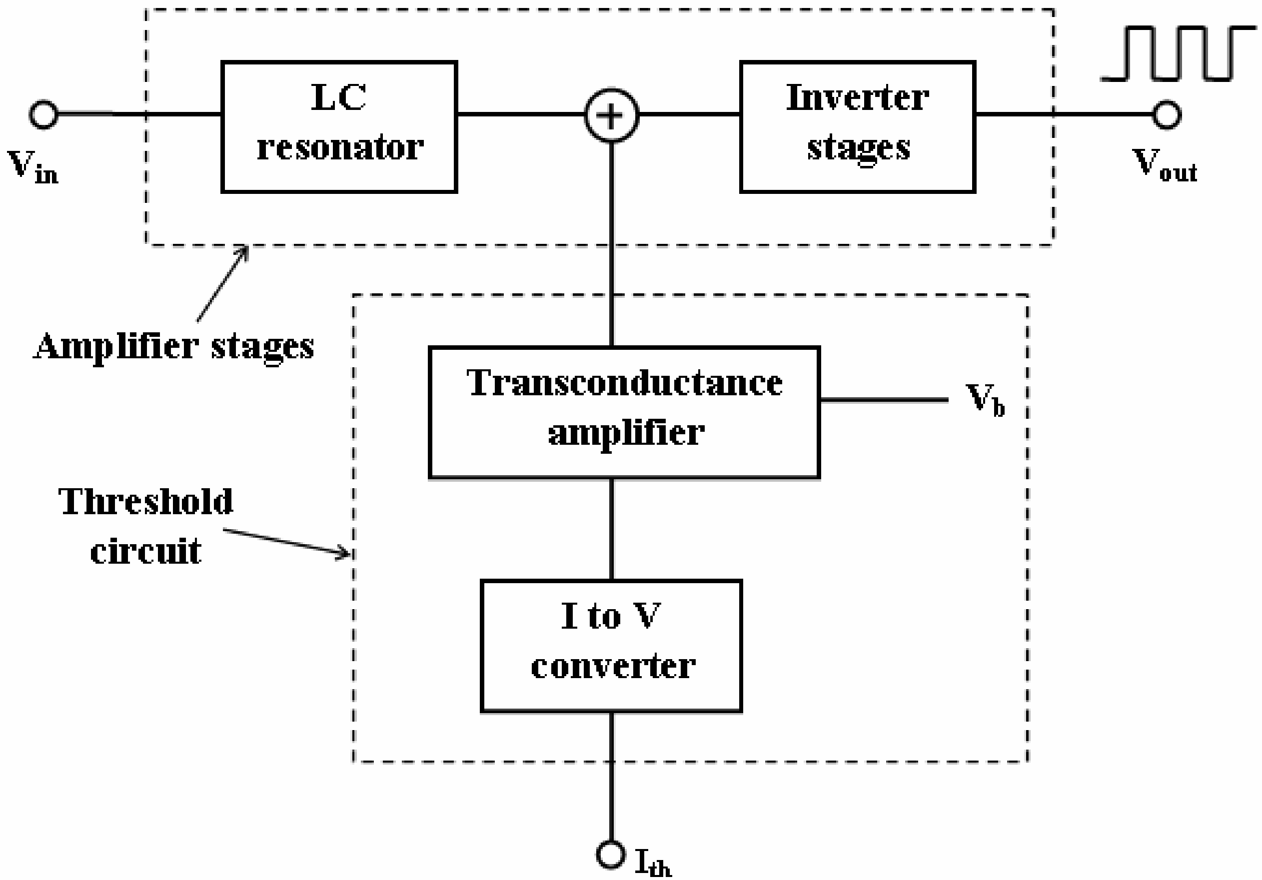
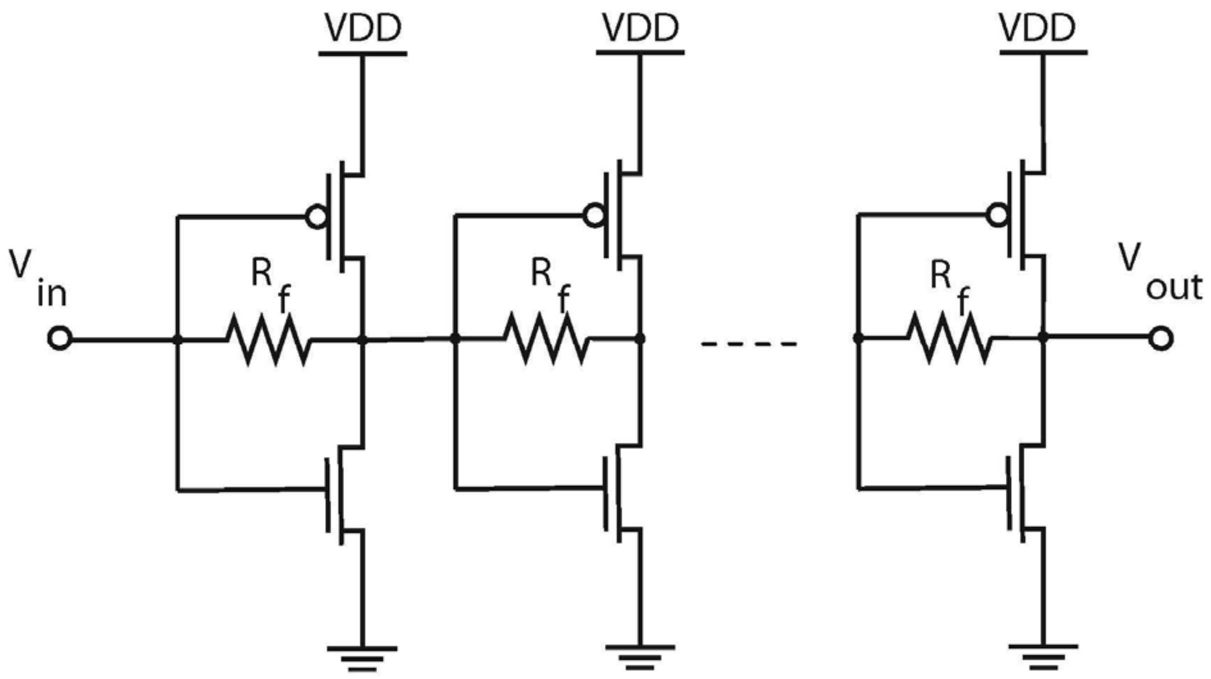
The proposed quantizer block diagram

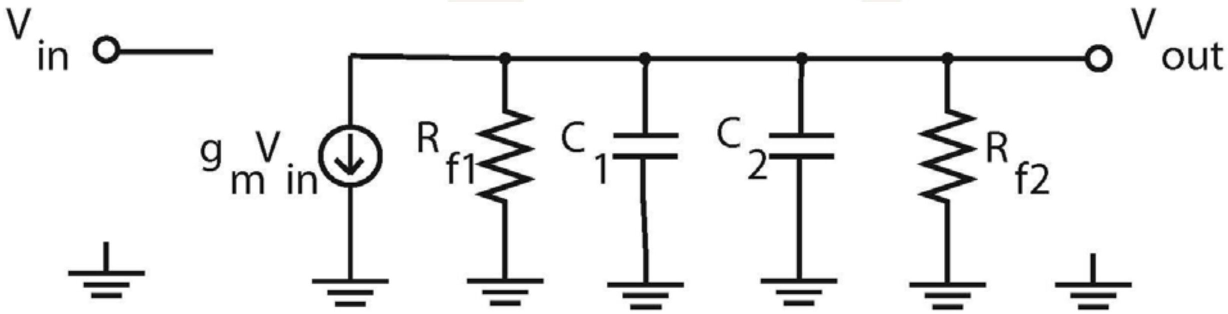


Amplifier stages (1)



- For increased bandwidth, strong feedback is applied sacrificing stage gain.
- Wider bandwidth is achieved at the expense of lower gain per stage by using low values of R_f

Amplifier stages (2)



Considering the inter-stage small signal model, the transfer function can be expressed as [7]:

$$\frac{V_{out}}{V_{in}} = \frac{-g_m R_T}{1 + sC_T R_T}$$

Where R_T denotes $R_{f1} \| R_{f2}$ and C_T represent $C_1 + C_2$
R_{f1} / R_{f2} and C_1 / C_2 denote equivalent resistors and capacitors contributed by previous and next stages, respectively.

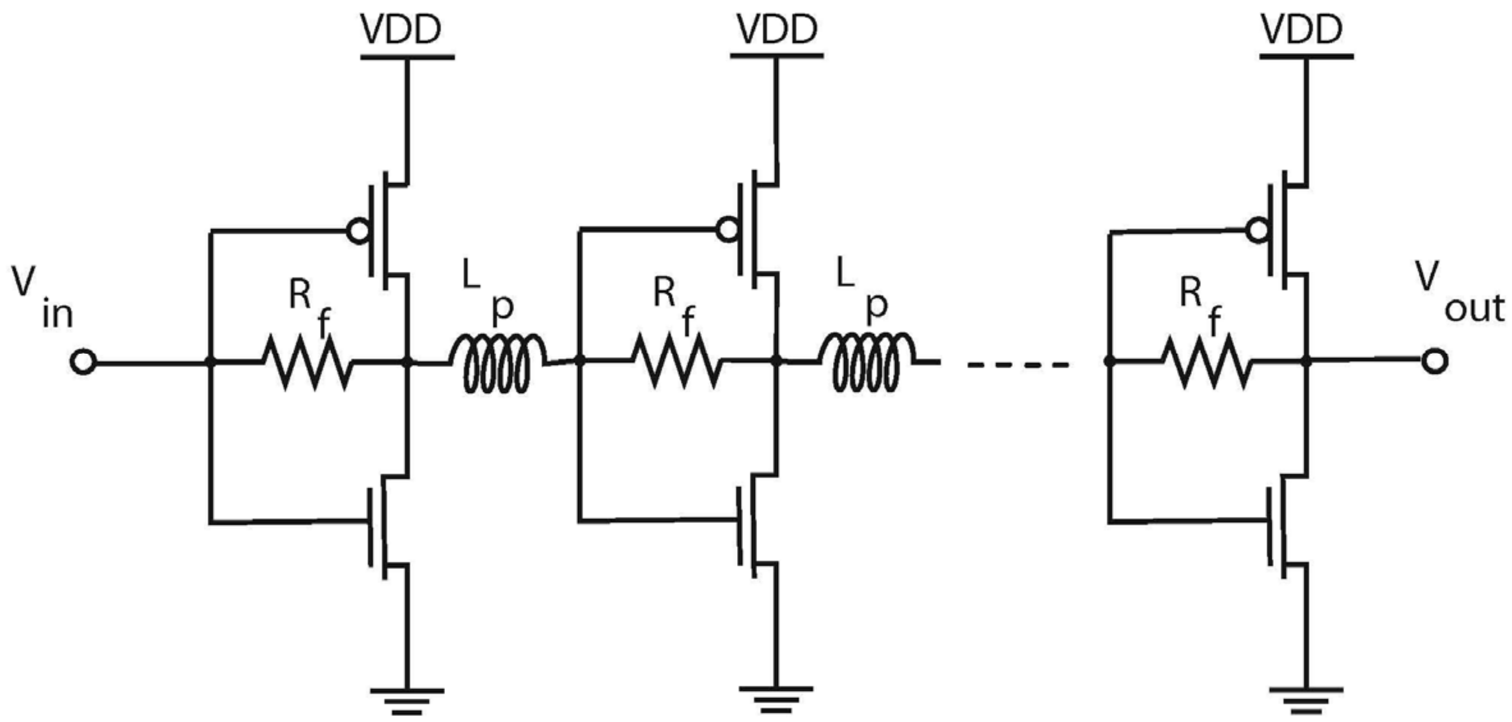
[7] C.-H. Wu, C.-H. Lee, W.-S. Chen, and S.-I. Liu, “Cmos wideband amplifiers using multiple inductive-series peaking technique,” IEEE Journal of Solid-State Circuit, vol. 40, no. 2, pp. 548–552, February 2005.

Disadvantage of using resitive feedback[8]

- Low gain
- Low output power
- Degraded noise figure

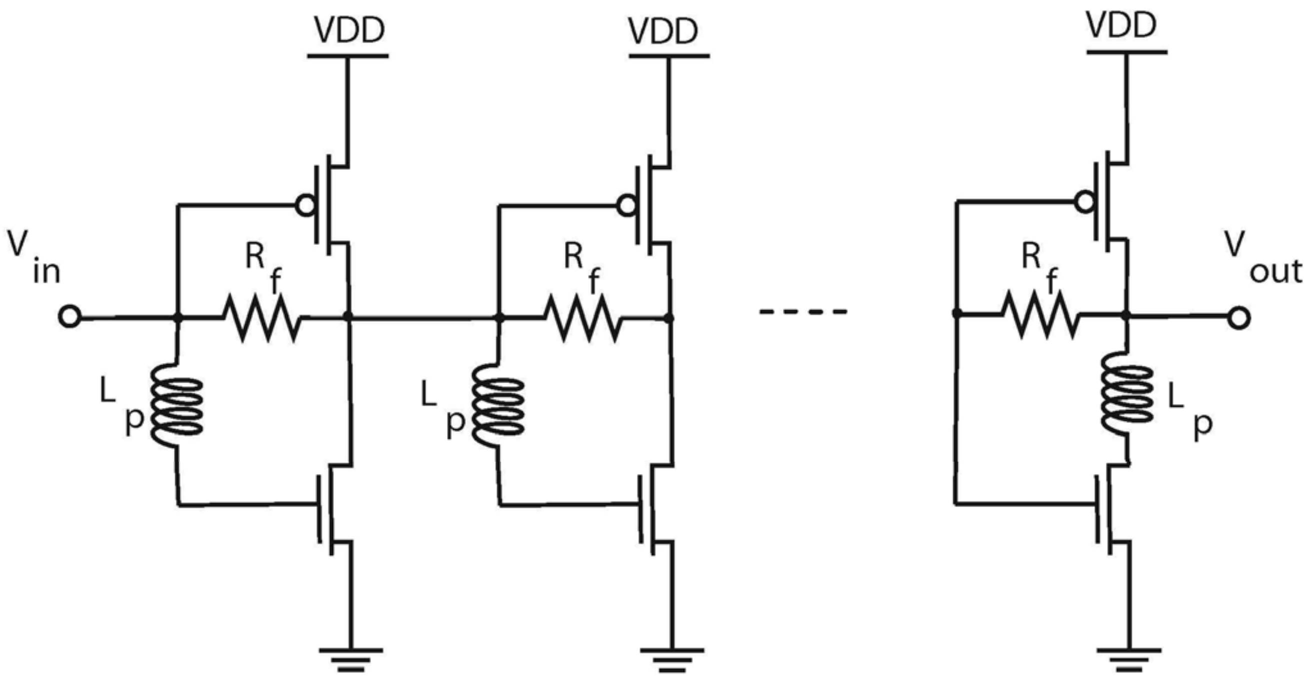
[8] R. Goyal, “High-frequency analog integrated circuit design,” in Willey Series in Microwave and Optical Engineering, 1995.

Multiple inductive-series peaking technique[7]



[7] C.-H. Wu, C.-H. Lee, W.-S. Chen, and S.-I. Liu, "Cmos wideband amplifiers using multiple inductive-series peaking technique," IEEE Journal of Solid-State Circuit, vol. 40, no. 2, pp. 548–552, February 2005.

Splitting-load inductive peaking technique[11]

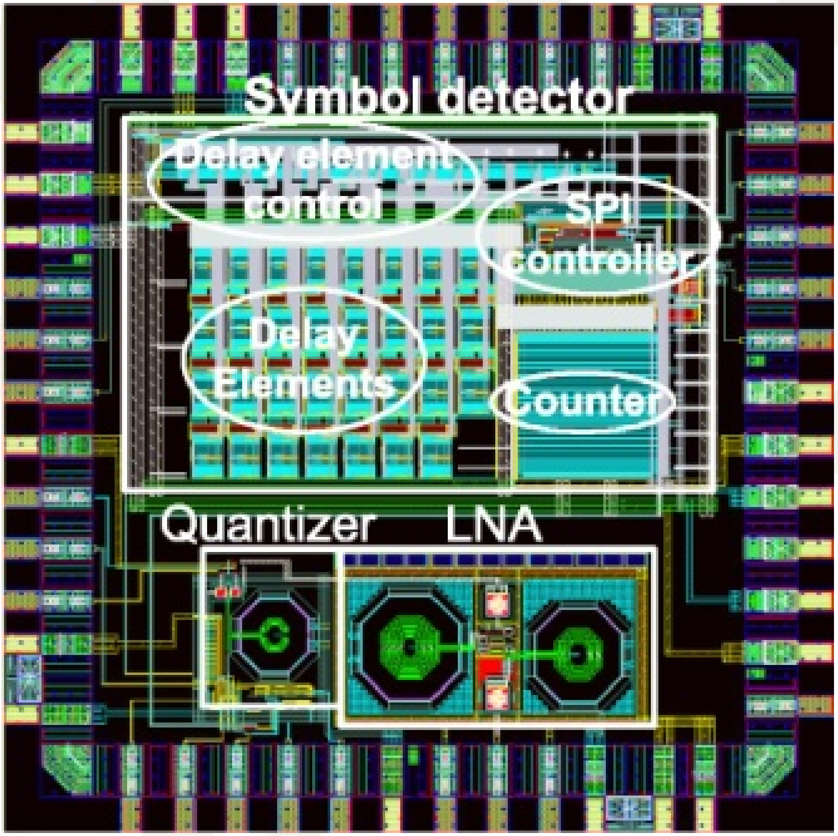


By locating a peaking inductor at the gate of nMOS of each inverter stage, the -3dB roll-off frequency can be boosted to higher frequencies.

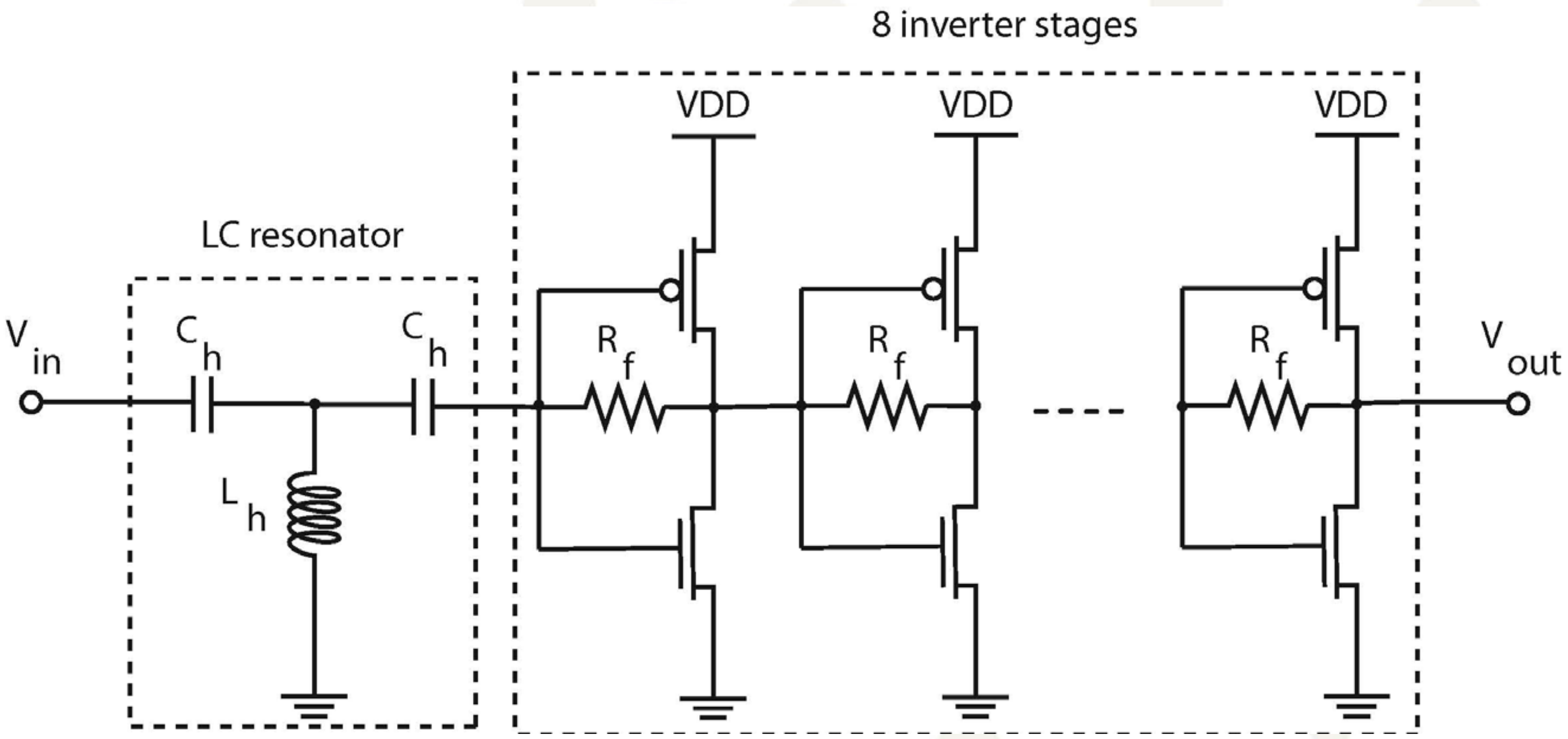
[11] S.-F. Chao, J.-J. Kuo, C.-L. Lin, M.-D. Tsai, and H. Wang, "A dc-11.5ghz low-power, wideband amplifier using splitting-load inductive peaking technique," IEEE Microwave and wireless components letters, vol. 18, no. 7, pp. 482–484, July 2008.

Disadvantage of using peaking inductors

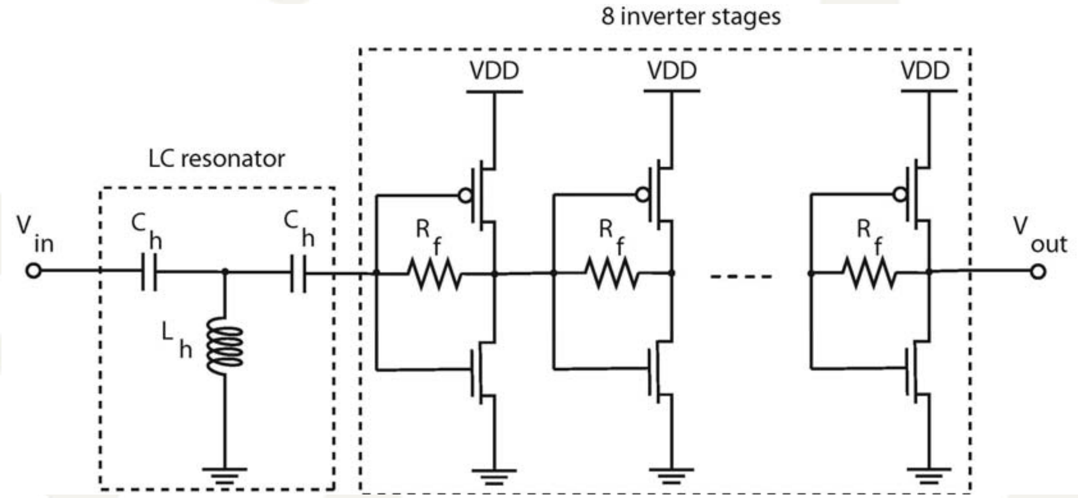
Area demanding



The proposed high-gain UWB amplifier



Advantage of the proposed solution

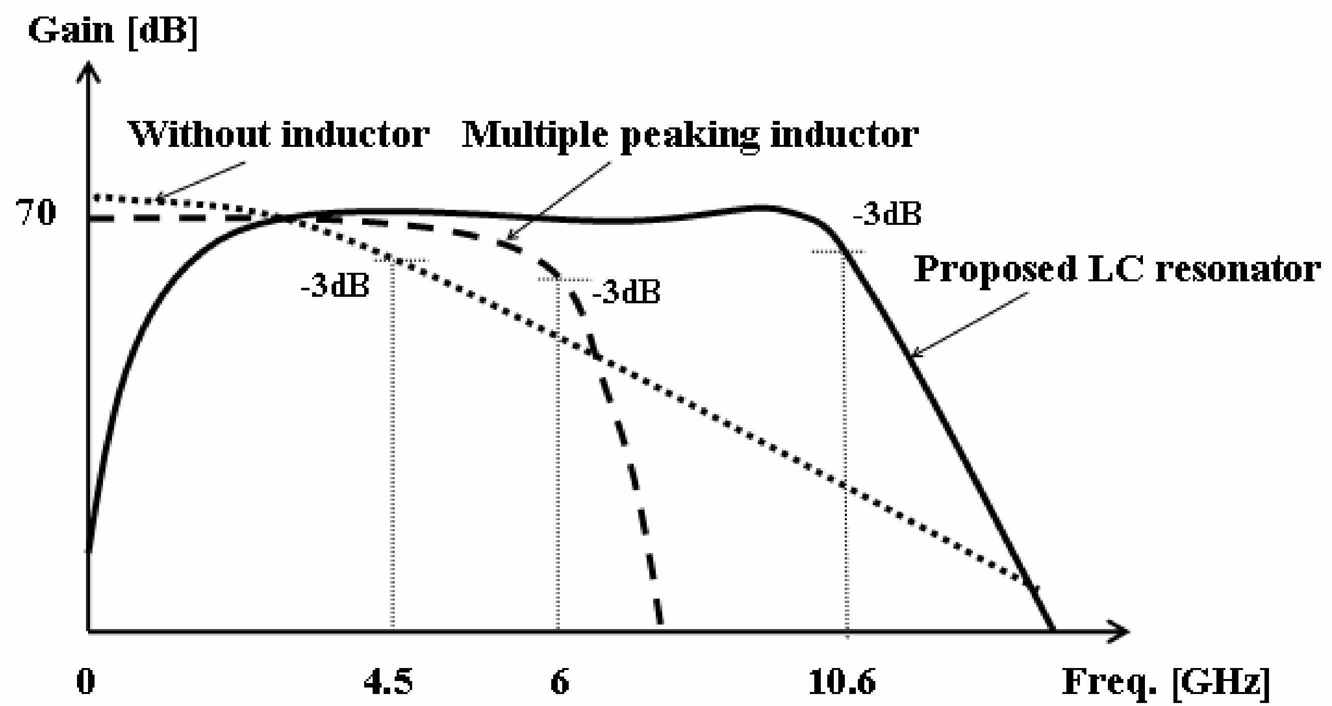


A resonant peak at the amplifier corner frequency can ’pull up’ the gain, thus extending the bandwidth significantly.

- A single, small inductor (0.82 nH) is used for the LC resonator regardless of the number of amplifier stages.

- The LC resonator also acts as a high-pass filter at the input, shifting the bandwidth to higher frequencies suitable for the FCC approved UWB spectrum.

Bandwidth comparison among the designs



Comparison with the state of the art

Design	TIA [7]	MMIC [11]	This Work
CMOS technology	0.18 µm	0.13 µm	90 nm
Supply voltage	1.8 V	1.3 V	1.2 V
Gain (dB)	61	13.2	70
-3 dB bandwidth	DC–7.2 GHz	DC–1.5 GHz	3.1 GHz–10.6 GHz
No. of stages	5	3	8
No. of inductors	8 (1.1 nH)	3 (2.4 nH, 2.4 nH, and 1.4 nH)	1 (0.82 nH)

[7] C.-H. Wu, C.-H. Lee, W.-S. Chen, and S.-I. Liu, “Cmos wideband amplifiers using multiple inductive-series peaking technique,” IEEE Journal of Solid-State Circuit, vol. 40, no. 2, pp. 548–552, February 2005.

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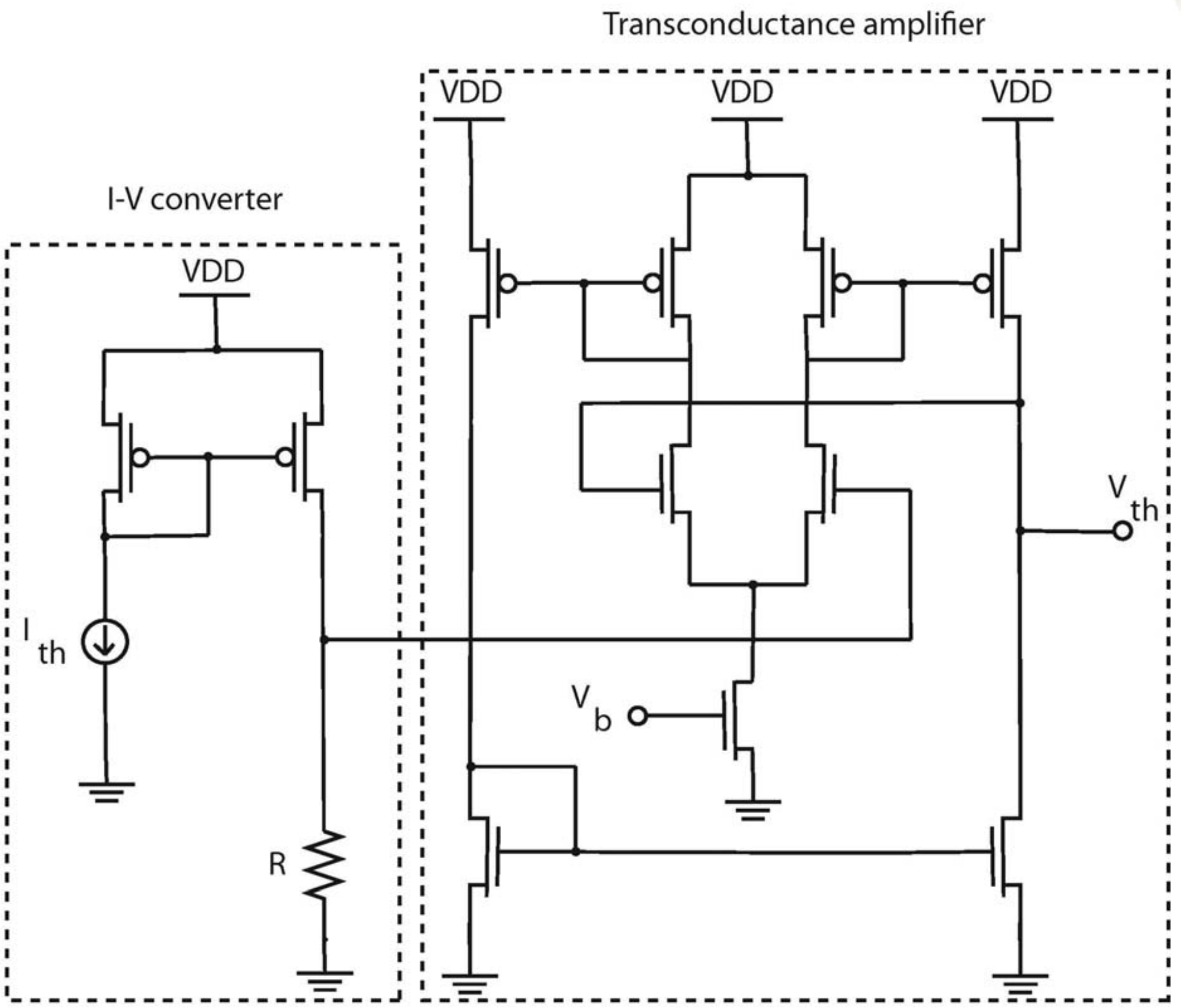
Threshold circuit



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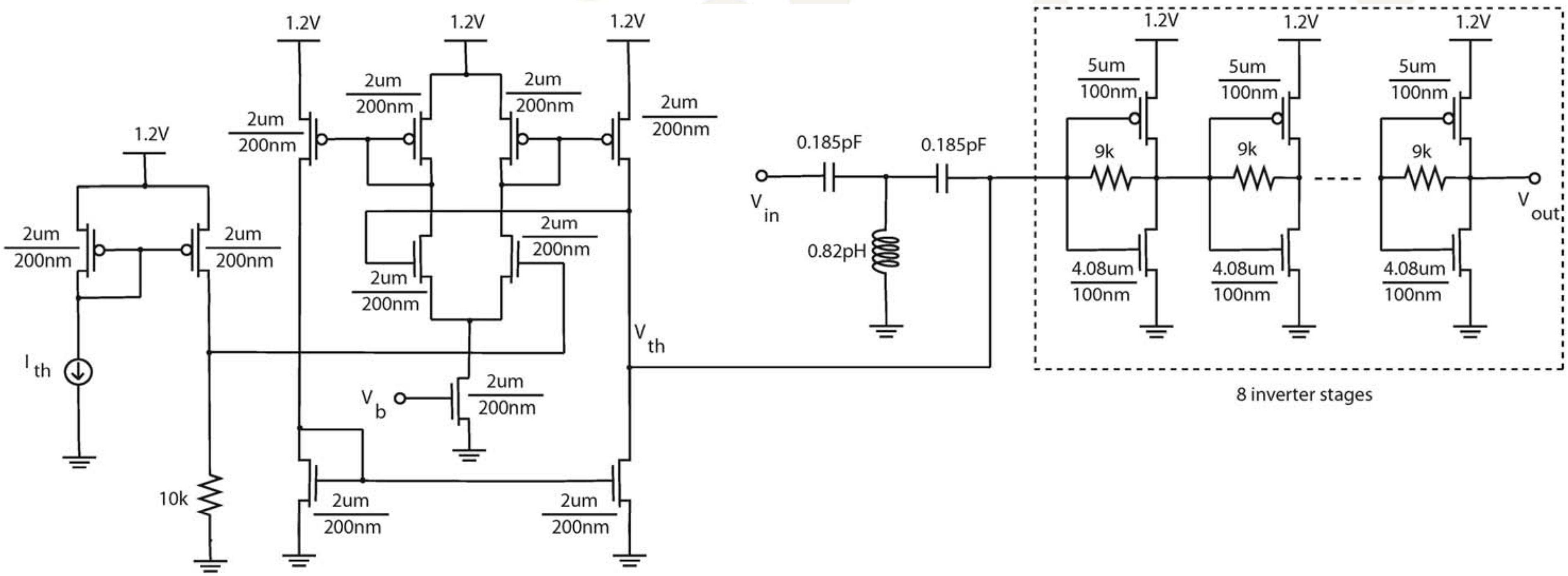
Simulated results (1)

• Simulated results of the quantizer for TSMC 90 nm CMOS technology are achieved using the CADENCE design environment.

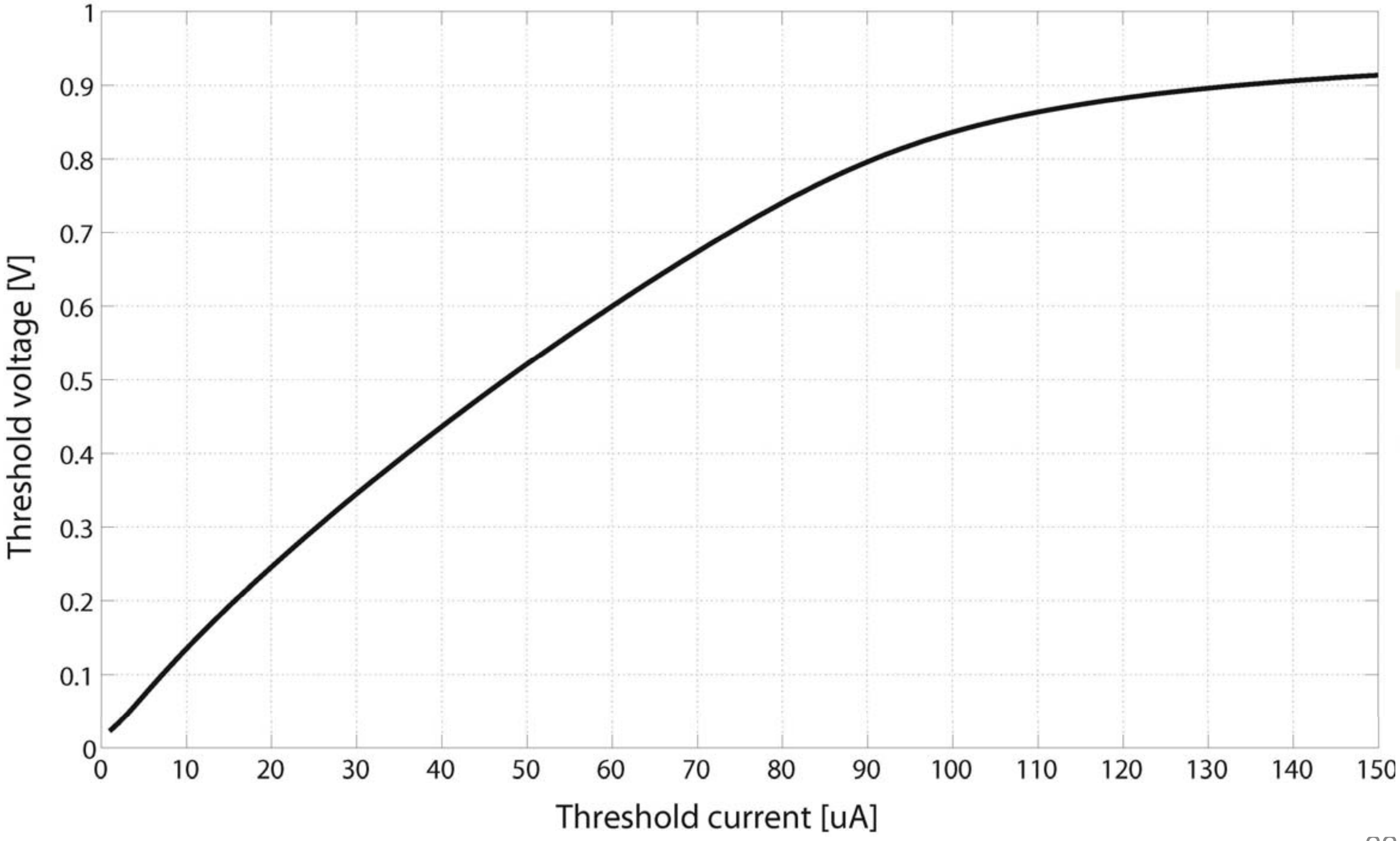
• All components used for simulation are RF models provided by TSMC.

Simulated results (2)



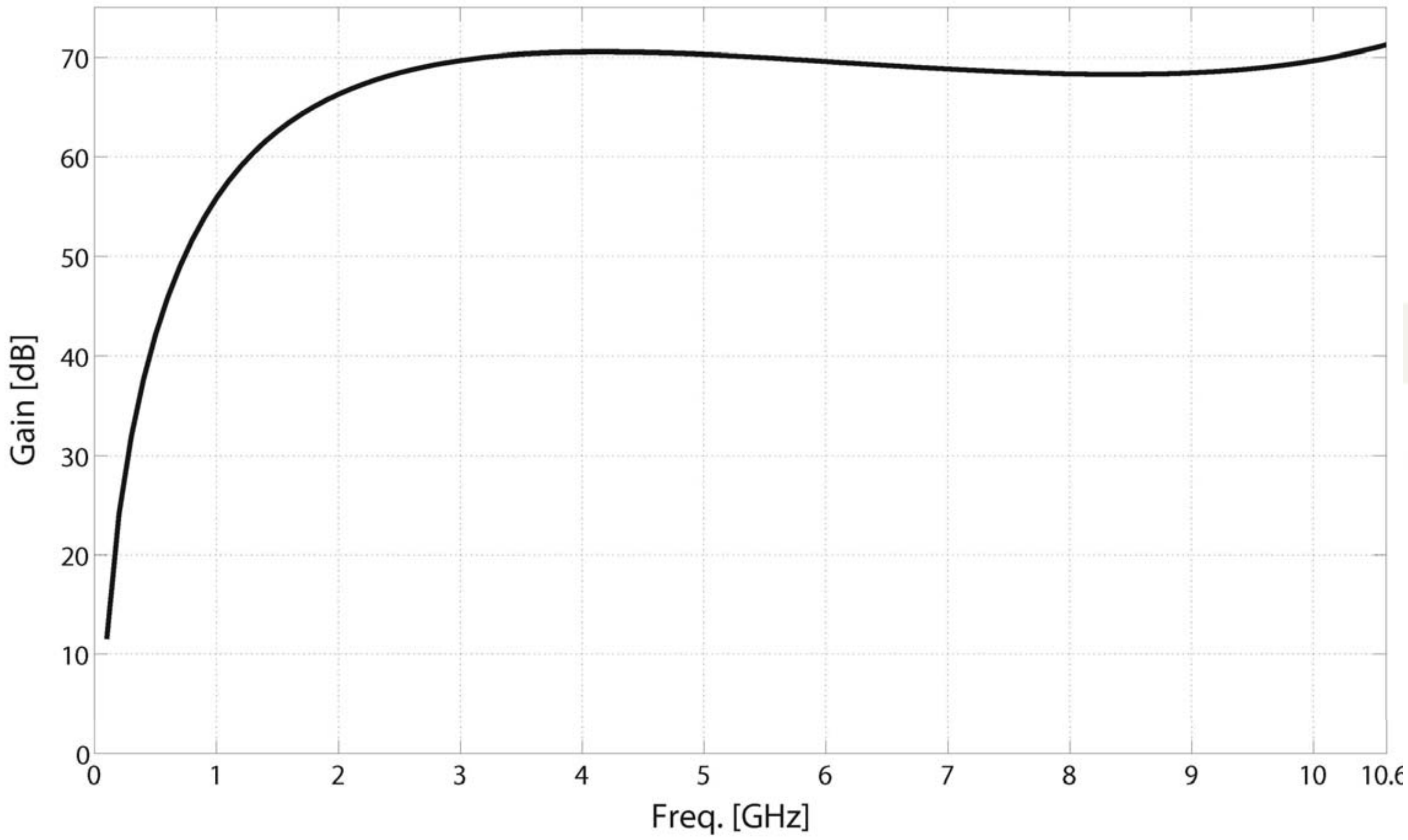
Simulated results (3)

The performance of the threshold circuit

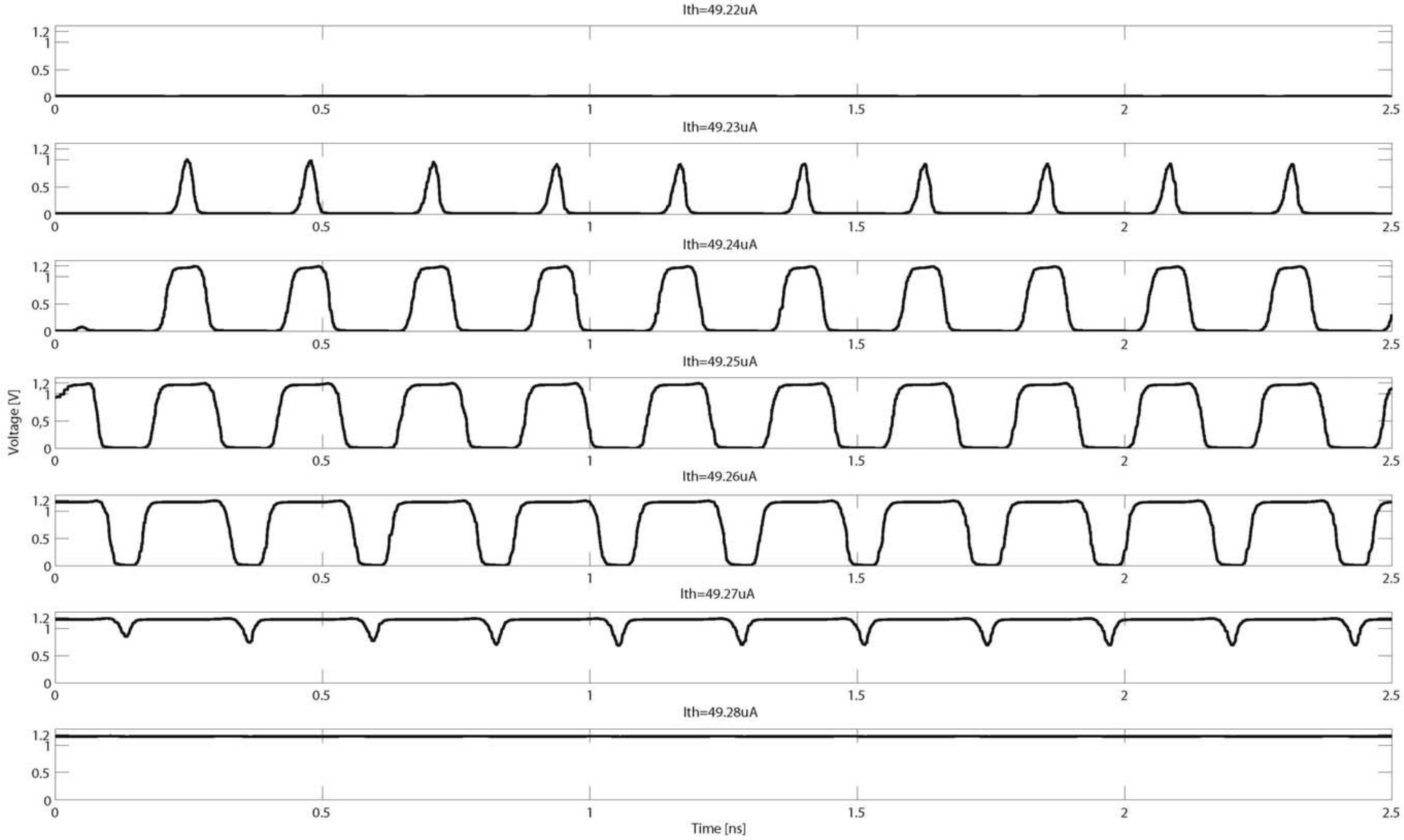


Simulated results (4)

Frequency response



Simulated results (5)



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Conclusions

• Proposing a continuous-time, ultra wideband quantizer with tunable threshold level and high gain suitable for FCC UWB applications

• The -3 dB bandwidth covering the entire FCC UWB spectrum from 3.1 GHz to 10.6 GHz.

• A very high gain of approximately 70 dB.

• Area-efficient, single-inductor solution designed for TSMC 90 nm CMOS technology.

References

[1] [Online]. Available: http://www.novelda.no/
[2] H. A. Hjortland and T. S. Lande, “CTBV integrated impulse radio design for biomedical applications,” IEEE Transactions on Biomedical Circuits and Systems, vol. 3, no. 2, pp. 79–88, Apr. 2009.
[3] H. A. Hjortland, D. T. Wisland, T. S. Lande, C. Limbodal, and K. Meisal, “Thresholded samplers for uwb impulse radar,” in IEEE International Symposium on Circuits and Systems, 2007. ISCAS 2007., 2007.
[4] Y. Li, K. Shepard, and Y. Tsividis, “A continuous-time programmable digital fir filters,” IEEE Journal of Solid-State Circuits, vol. 41, no. 11, pp. 2512–2530, Nov. 2006.
[5] B. Schnell and Y. Tsividis, “A continuous-time adc/dsp/dac system with no clock and with activity-dependent power dissipation,” IEEE Journal of Solid-State Circuits, vol. 43, no. 11, pp. 2472–2481, Nov. 2008.
[6] B. Goll and H. Zimmermann, “A 65nm cmos comparator with modified latch to achieve 7ghz/1.3mw at 1.2v and 700mhz/47uw at 0.6v,” pp. 328–329, February 2009.
[7] C.-H. Wu, C.-H. Lee, W.-S. Chen, and S.-I. Liu, “Cmos wideband amplifiers using multiple inductive-series peaking technique,” IEEE Journal of Solid-State Circuit, vol. 40, no. 2, pp. 548–552, February 2005.
[8] R. Goyal, “High-frequency analog integrated circuit design,” in Willey Series in Microwave and Optical Engineering, 1995.
[9] R. Schaumann and M. Valkenburg, “Design of analog filters,” in New York: Oxford Univ. Press, 2001.
[10] S. Galal and B. Razavi, “A 40gb/s amplifier end esd protection circuit in 0.18um cmos technology,” in IEEE International Solid-State Circuits Conference (ISSCC) Dig. Tech. Papers, February 2004, pp. 480–481.
[11] S.-F. Chao, J.-J. Kuo, C.-L. Lin, M.-D. Tsai, and H. Wang, “A dc-11.5ghz low-power, wideband amplifier using splitting-load inductive peaking technique,” IEEE Microwave and wireless components letters, vol. 18, no. 7, pp. 482–484, July 2008.

THANK YOU FOR YOUR ATTENTION!

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