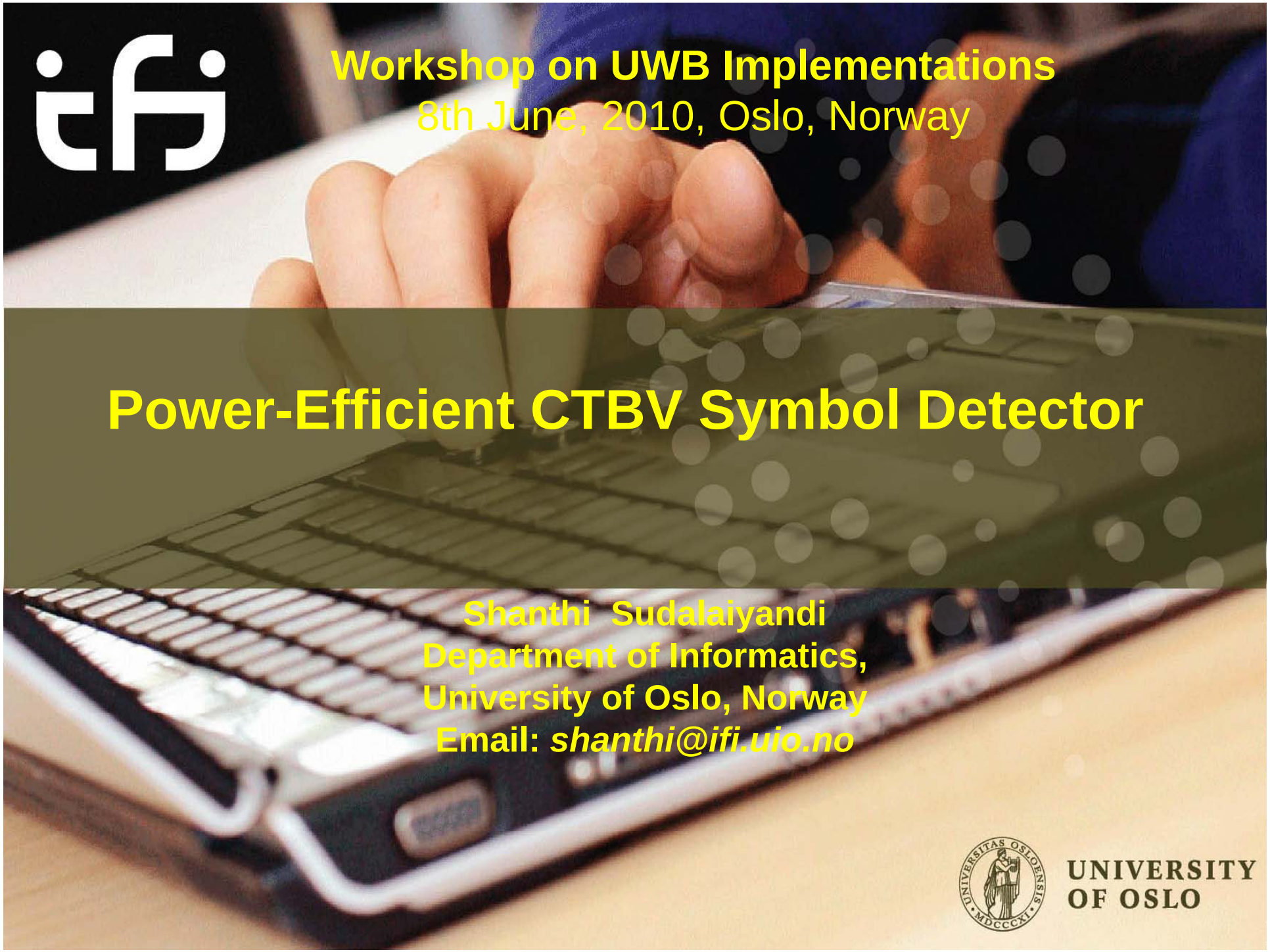

Workshop on UWB Implementations
8th June, 2010, Oslo, Norway

Power-Efficient CTBV Symbol Detector

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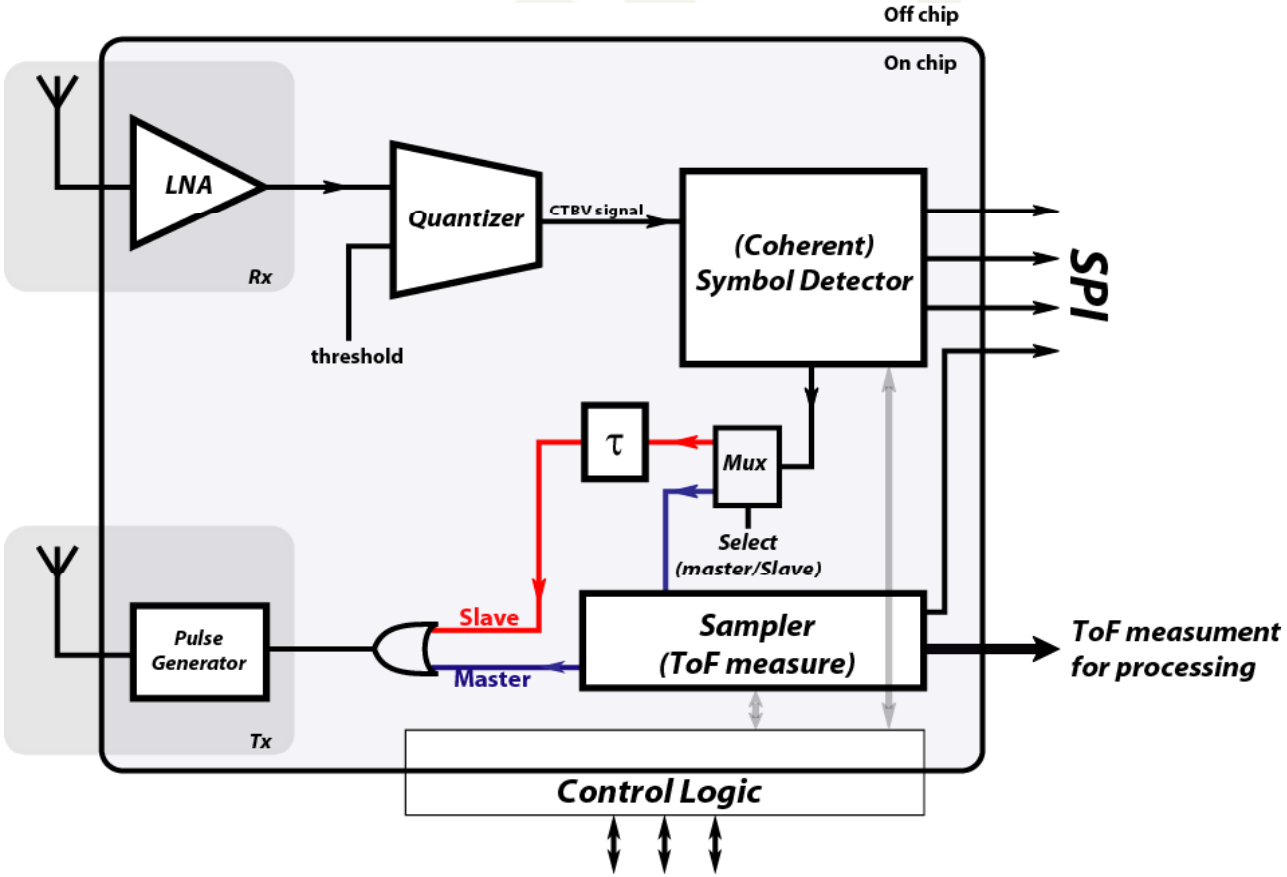
Outline

1. Introduction
2. UWB Symbol detector Architecture
3. Simulated results
4. Conclusion

Introduction

- Melody chip - Active Echo Engine



Introduction contd..

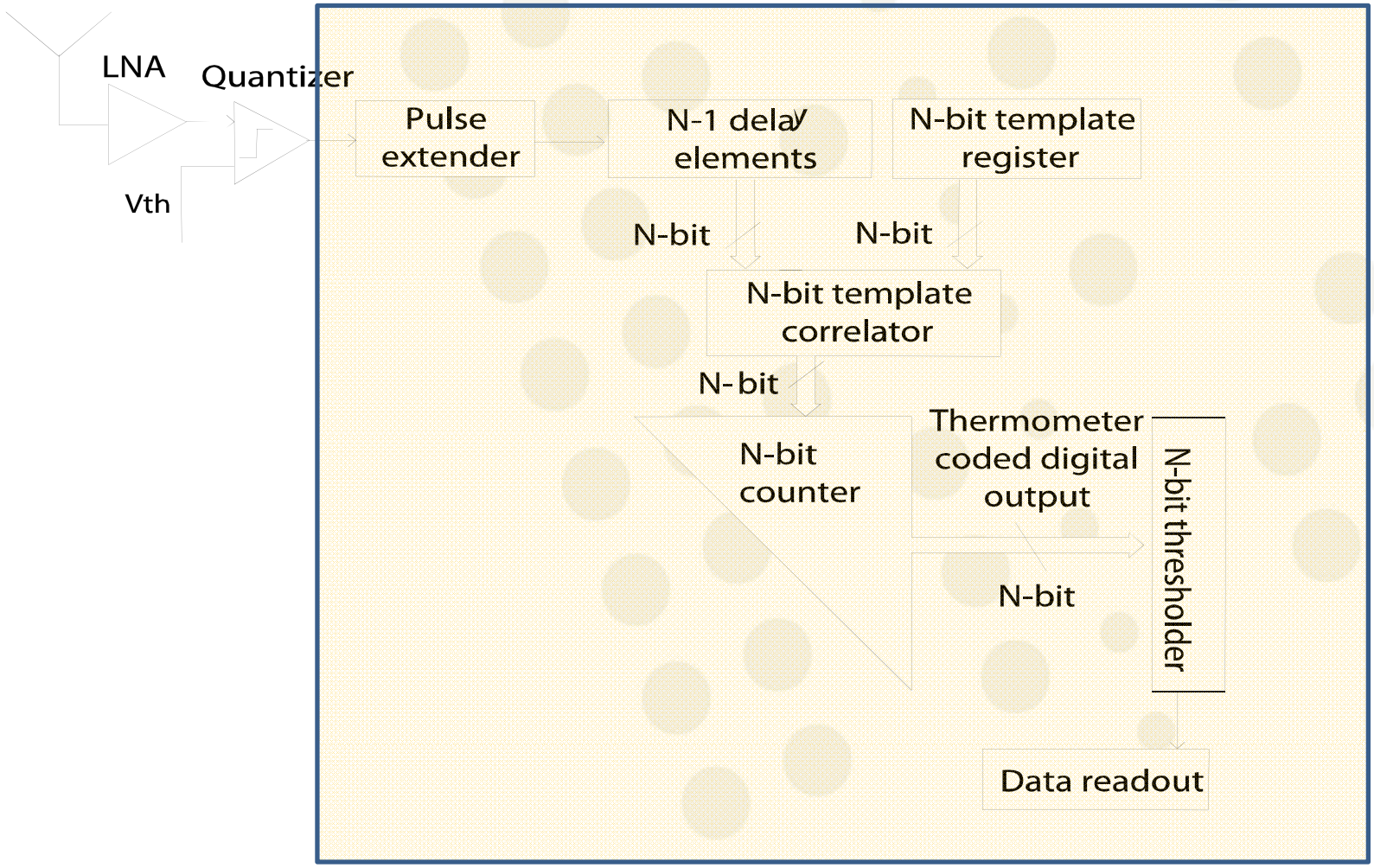
Problem statement:

- Accurate synchronization and high resolution clocks are major obstacle for a power efficient CMOS solution.
- Most implementations tradeoff performance for low complexity operation.

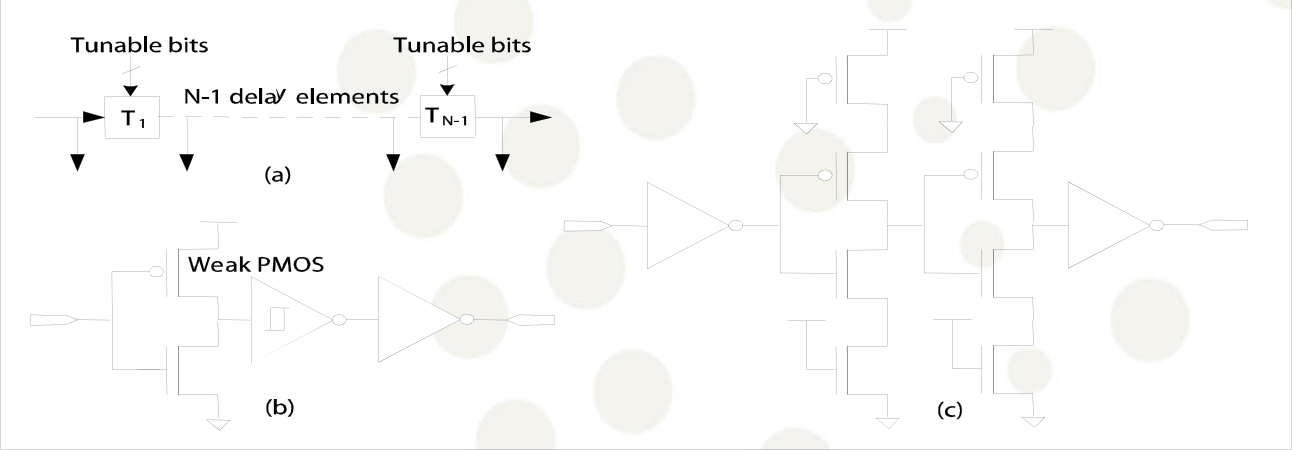
Proposed solution:

- A novel coherent symbol detector architecture using time-domain running cross-correlation.
- Combination of CTBV coding and unique combinational circuits in standard CMOS.
- A clockless power-efficient solution leading to high sensitivity receiver .

UWB Symbol detector architecture

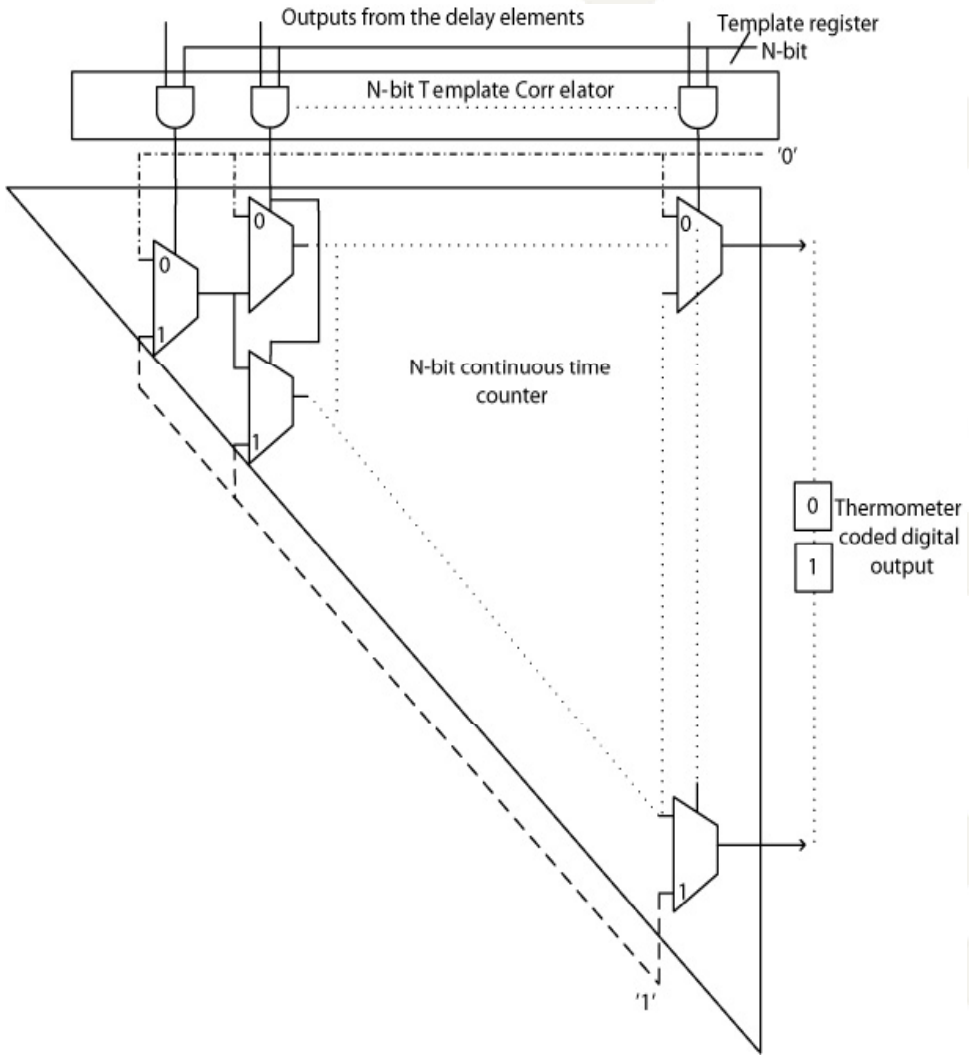


Details of processing blocks



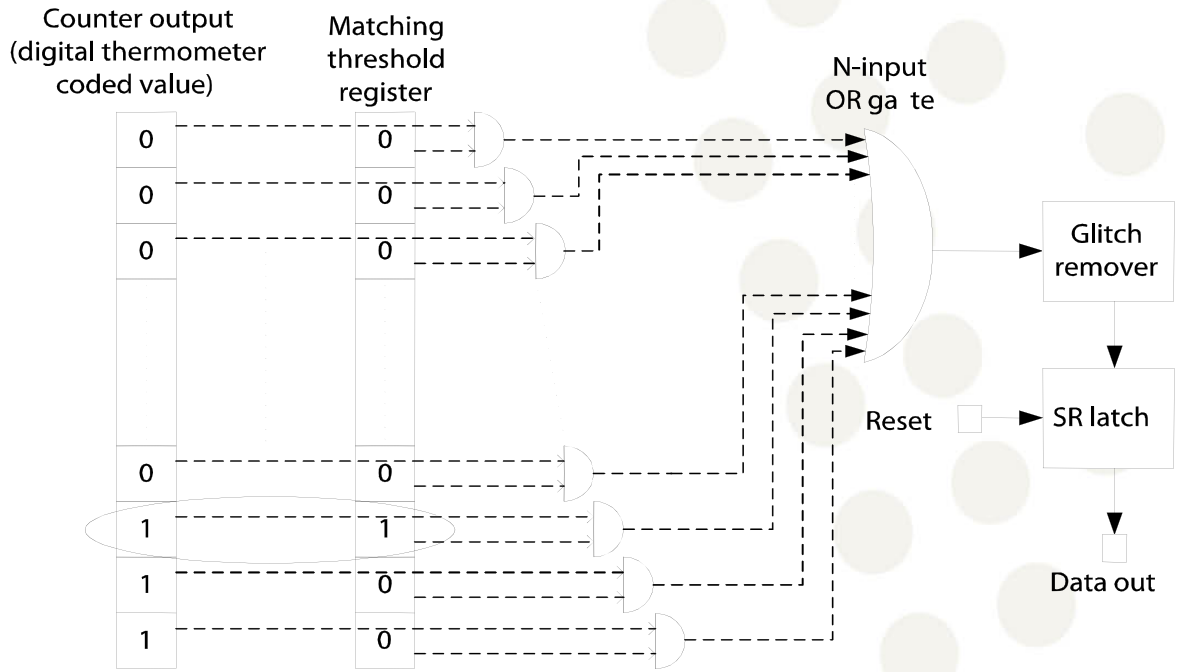
- (b) Pulse extender
  - A tunable pulse extender for the incoming signal up to ~3ns.
- (a) Delay elements
  - A 32-bit programmable delay line equivalent to the chip-rate.
  - Each delay element consists of a coarse tune and a fine tune.
- (c) Coarse delay element
  - Cascaded NMOS and PMOS structure gives increased delay with minimal area overhead.

N-bit continuous time counter



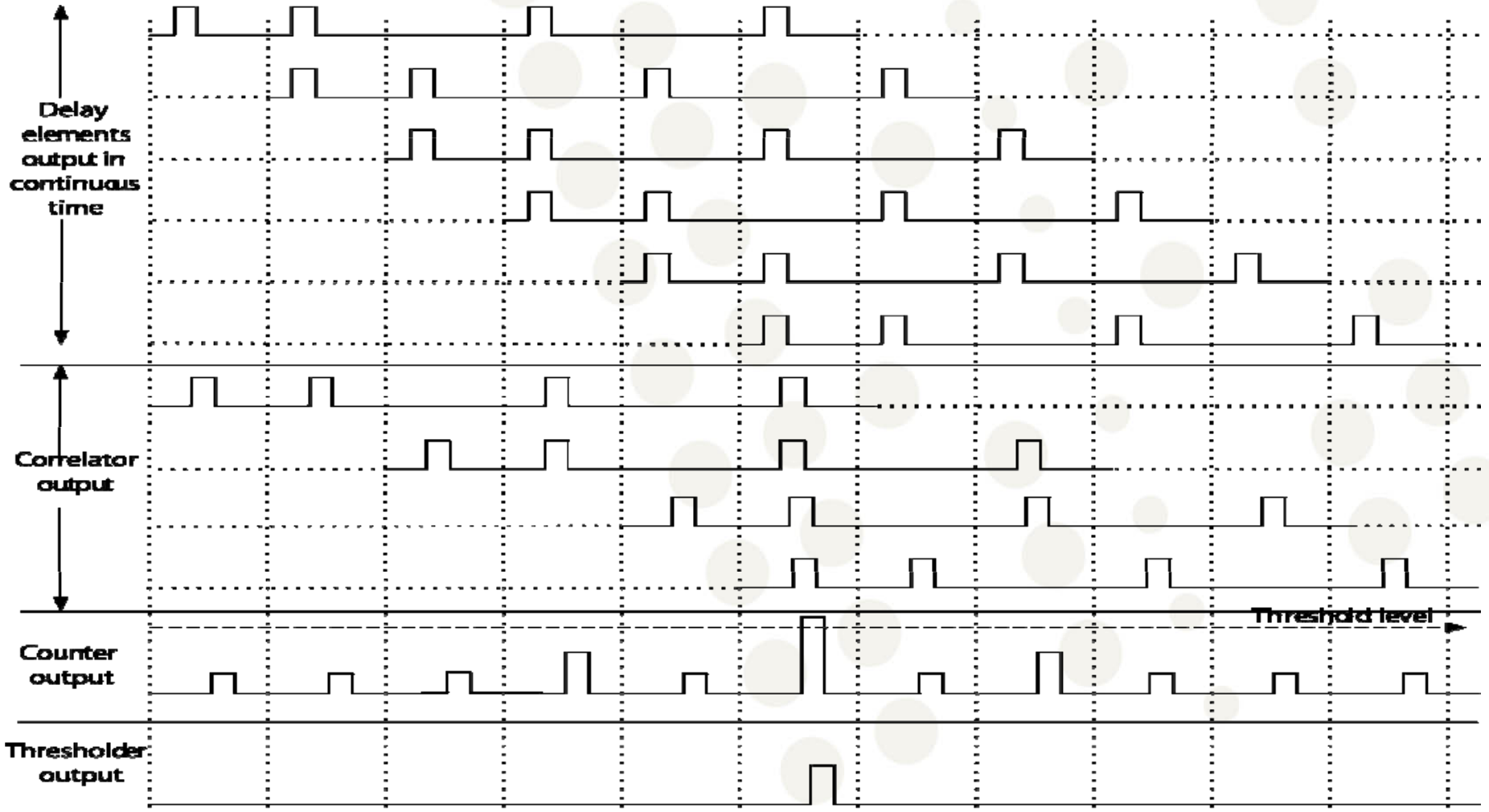
- Correlator detects the occurrence of pulses (bit ‘1’) in the incoming signal.
- Novel N-bit continuous time counter counts the pulses.
- The counter output is a thermometer coded digital value.

N-bit thresholder

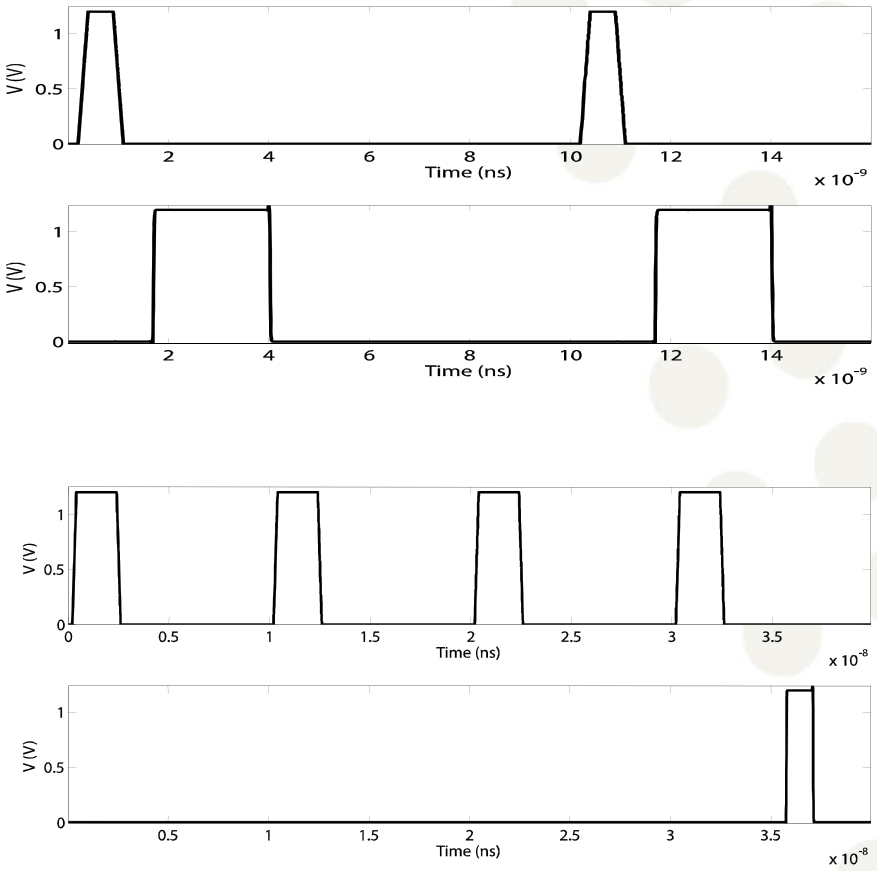


- Thresholder compares the counter output with the matching threshold register for symbol detection.
- Statistical symbol detection with appropriate threshold setting.
- Any undesired glitches are removed through the glitch remover circuit.

Symbol generation principle



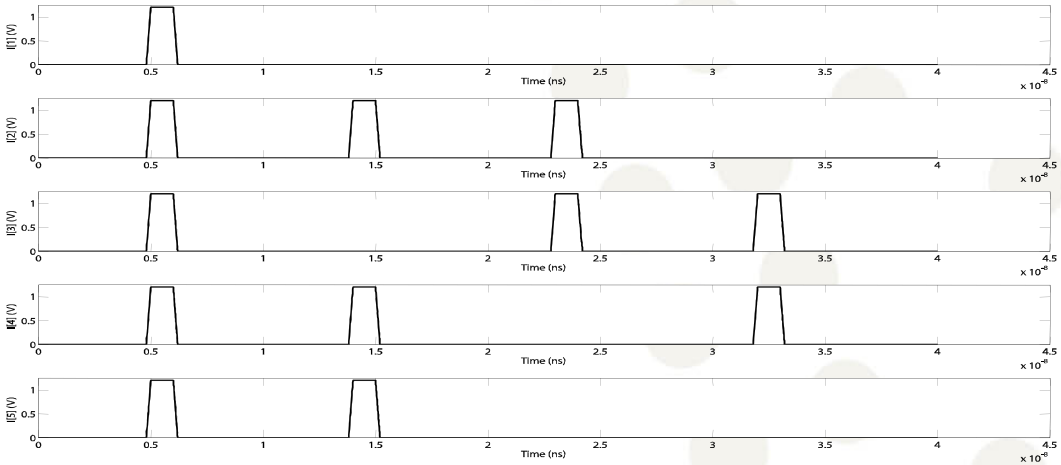
Simulation results

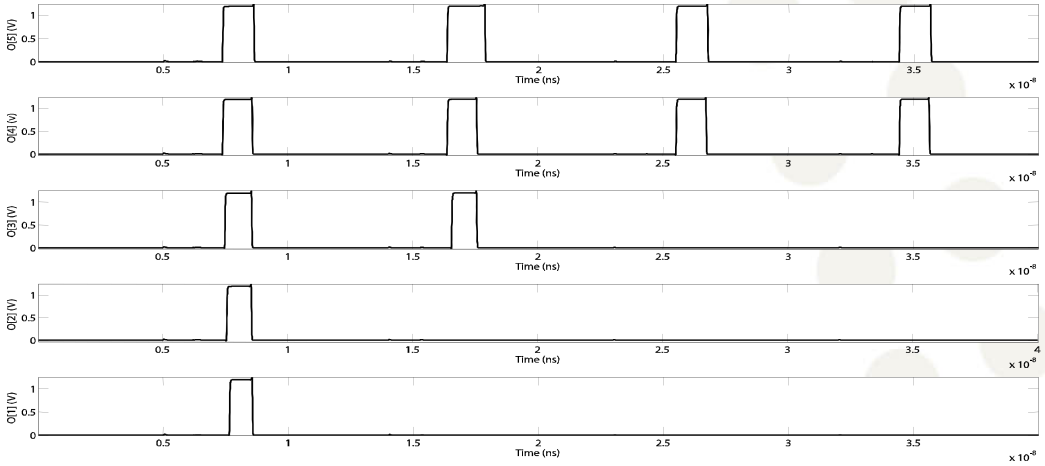


- Post layout simulation in 90nm TSMC low power process technology.

- Simulation results of the pulse extender circuit and a delay element block.

Simulation results contd.

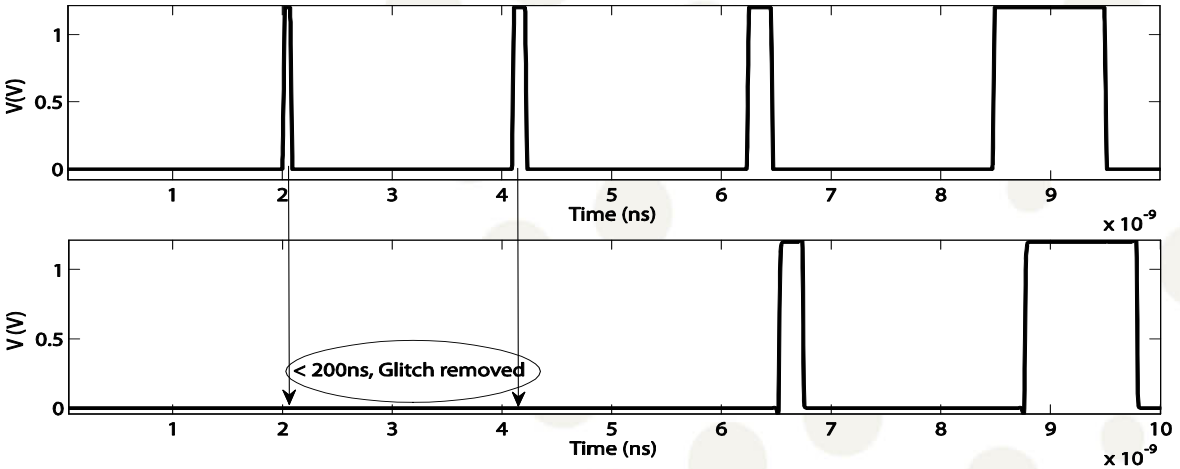




- Simulation results of the counter input shown for 5-bits.

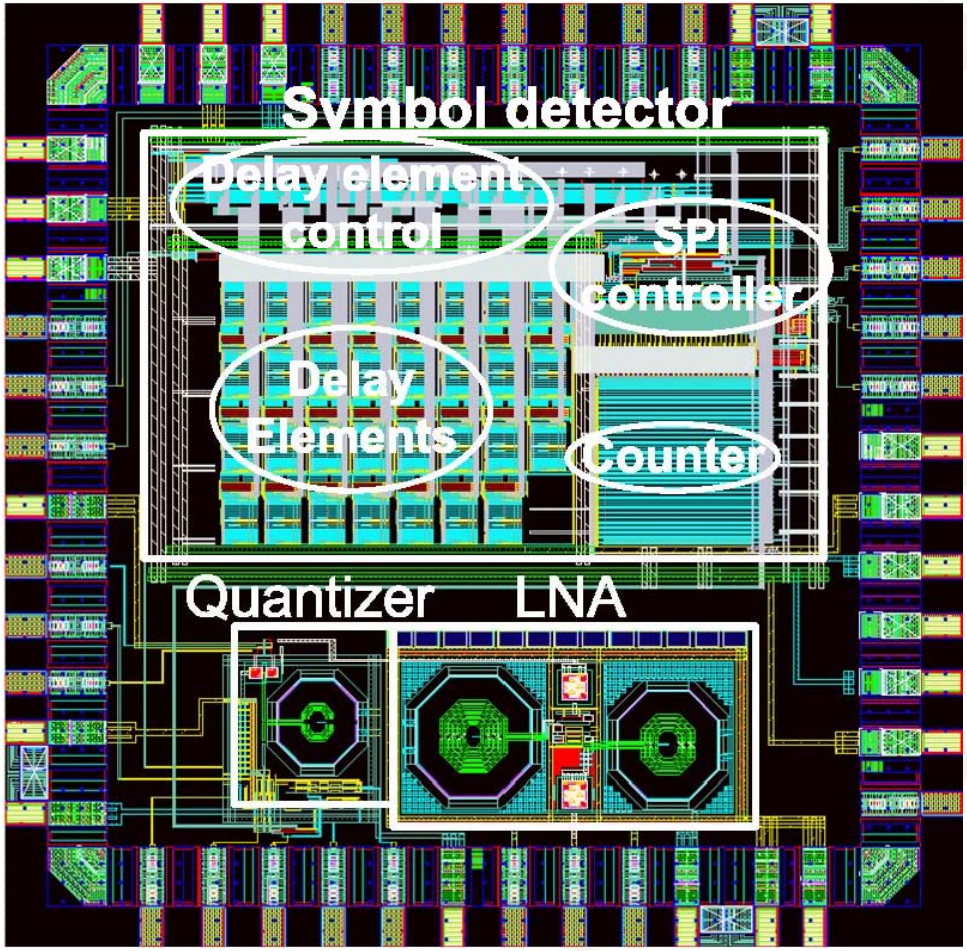
- Simulation results of the counter output showing the thermometer coded digital output

Simulation results contd.



- Simulation results of the glitch remover.
- Any pulses less than 200ns are removed.

Melody Chip


Symbol detector
Delay element control
SPI controller
Delay Elements
Counter
Quantizer
LNA

Conclusion

- Proposed a novel coherent symbol detector for power-efficient implementation in standard CMOS.

- A simple solution to achieve high sensitivity receiver for accurate ToF measurement.

- Post layout simulations in TSMC 90 nm CMOS technology validates the proposed architecture.

- We got the chip now and in the process of calibration and measurement to verify the performance of the symbol detector.

- Paper to be presented in ICUWB 2010 conference.

THANK YOU