LNA design in CMOS for 10 GHz bandwidth

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LNA design in CMOS for 10 GHz bandwidth

- Challenges in the design of LNAs with bandwidth towards 10 GHz
- Implemented circuit
- Measurements

LNA design in CMOS for 10 GHz bandwidth

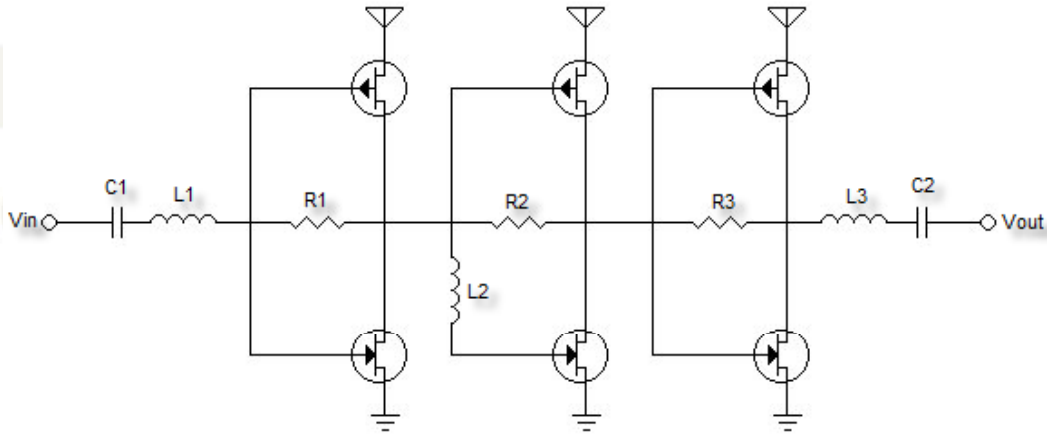
- Challenges in the design of LNAs with bandwidth towards 10 GHz
  - Lower supply voltage → Fewer topologies
  - Matching and bandwidth enhancement with as few inductors as possible
  - Lower dynamic range → Lower SNR

LNA design in CMOS for 10 GHz bandwidth

- Challenges in the design of LNAs with bandwidth towards 10 GHz
- **Implemented circuit**
  - PLS performance
  - Matching properties
- Measurements

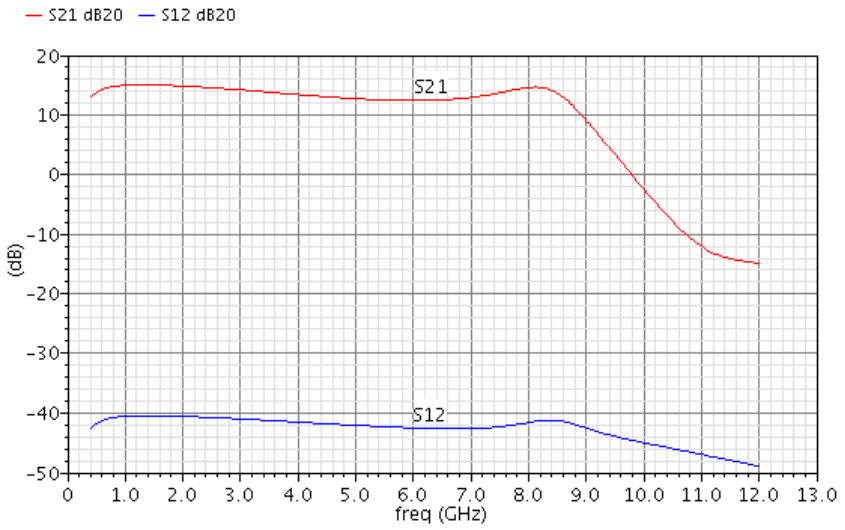
LNA design in CMOS for 10 GHz bandwidth

- Implemented circuit
  - Inverter based
  - Splitting -load peaking stage
  - Implemented without bond wire model



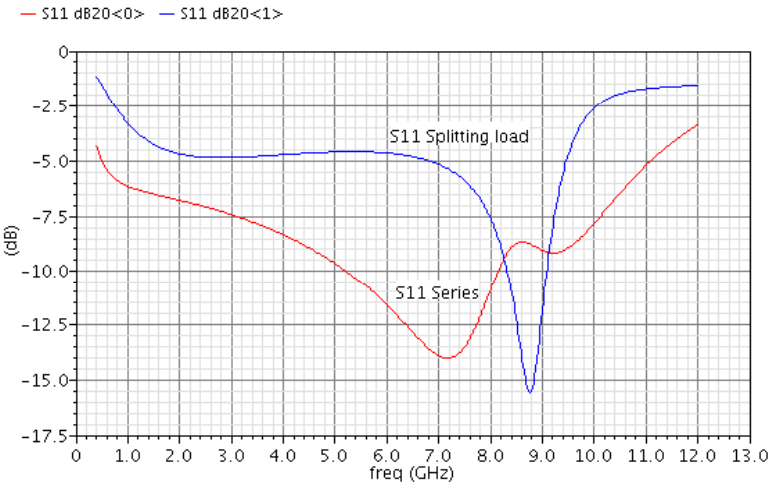
LNA design in CMOS for 10 GHz bandwidth

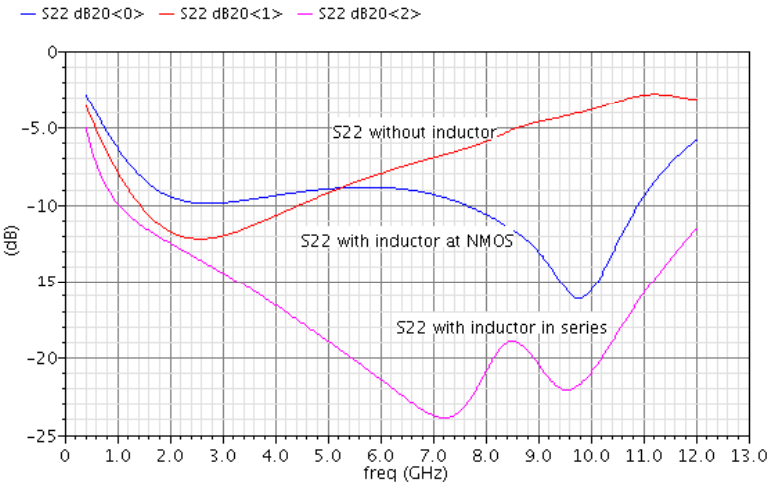
- Implemented circuit
  - S21 15.1 dB
  - Bandwidth 0.4-8.6 GHz
  - NF < 5.8 dB



LNA design in CMOS for 10 GHz bandwidth

- Implemented circuit
  - Matching approaches



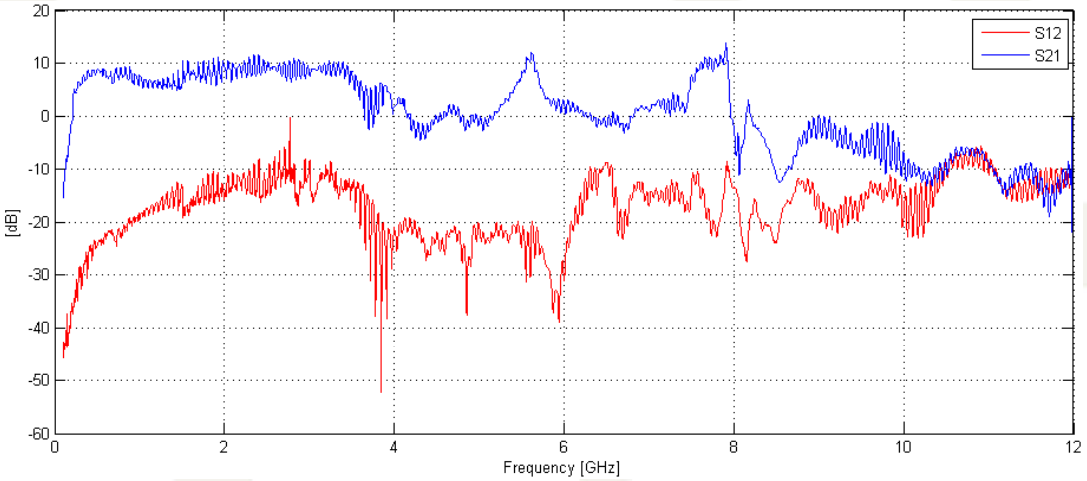


LNA design in CMOS for 10 GHz bandwidth

- Challenges in the design of LNAs with bandwidth towards 10 GHz
- Implemented circuit
- **Measurements**
  - Results
  - Reasons for degradation

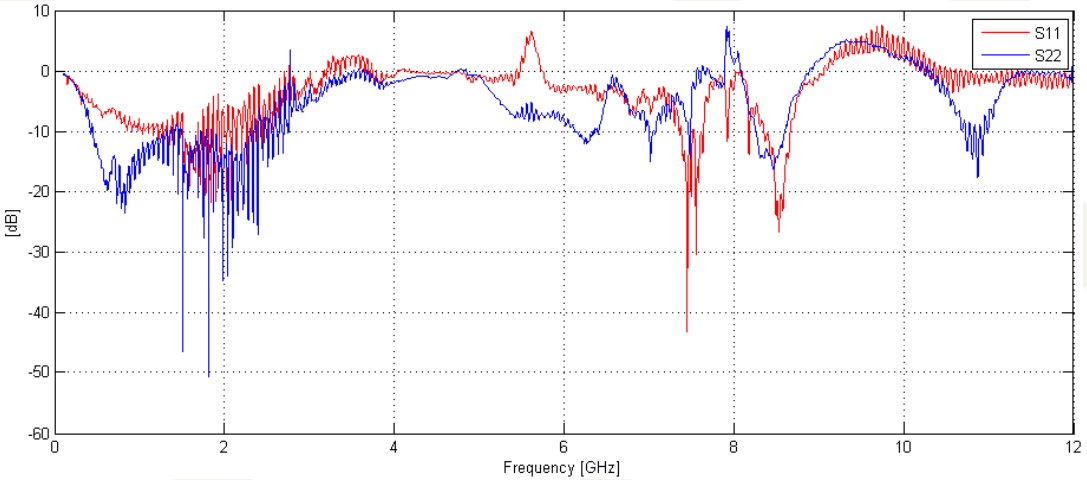
LNA design in CMOS for 10 GHz bandwidth

- Measurements
  - Gain 9.5±2dB between 0.3 and 3.6 GHz
  - Reverse gain 30 dB higher than PLS
  - “Spiky” responses



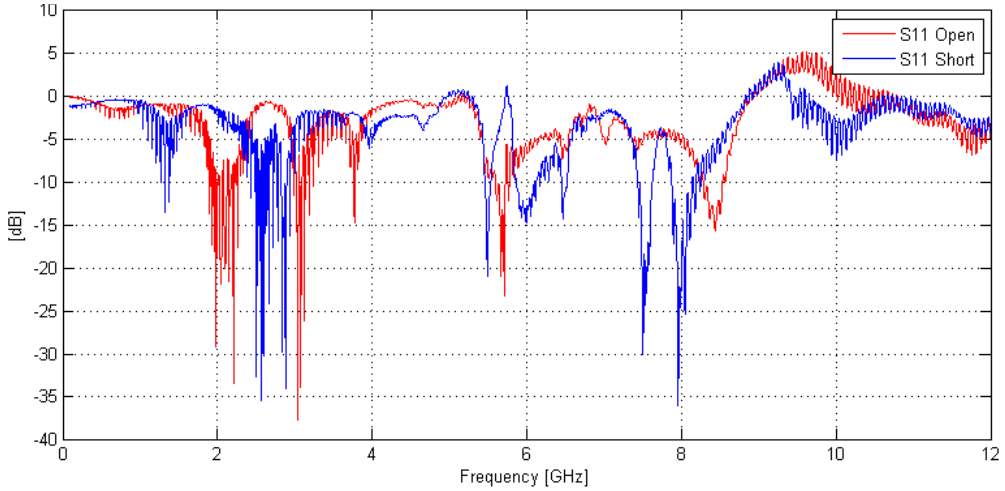
LNA design in CMOS for 10 GHz bandwidth

- Measurements
  - S11 and S22
  - Total reflection in large parts of the sweep



LNA design in CMOS for 10 GHz bandwidth

- Measurements
  - Open and shorted bond wire test benches included
  - Resonates at above 9 GHz



LNA design in CMOS for 10 GHz bandwidth

- Measurement,
  reasons for degradation from PLS to measurements

  – Reactive nature of bond wire and pad degrades matching properties
  – S12 results indicate cross talk on PCB
  – Noisy measurement environment

LNA design in CMOS for 10 GHz bandwidth

- Summary:
  - LNA design in CMOS for 10 GHz is a challenge
    - Reducing the number of inductors, still achieve the bandwidth and matching properties
    - Maintaining the simulated performance from PLS to measurements
  - Good models of bond wire and pad are essential to implement in the design phase for a good results

LNA design in CMOS for 10 GHz bandwidth

- References:

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