Stochastic Resonance IR-UWB Communications Receiver

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Bitstreams

Bitstreams:

- Bitstreams are well suited for fast processing in CMOS
- Arithmetic operations can be just single gates

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Stochastic resonance

Stochastic resonance:

- When the SNR is low, each analog sample of the signal might contain less than one bit of information
- 1 bit quantization is sufficient. Little information is lost during quantization.
- Integrate to get higher SNR
- We call this stochastic resonance
- Analog averaging vs. stochastic resonance averaging: Approx. 2 dB loss.

Stochastic resonance principle.

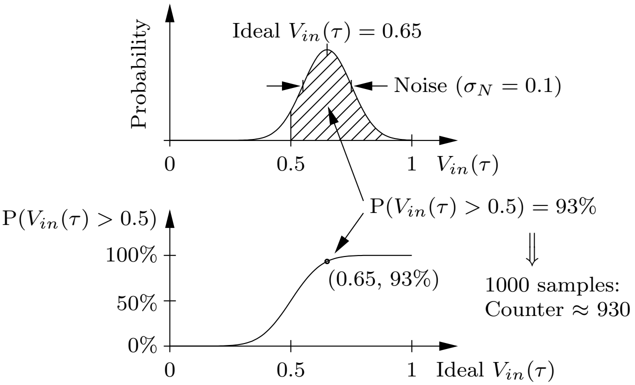

Figure: Stochastic resonance principle.

Stochastic resonance integration PMF.

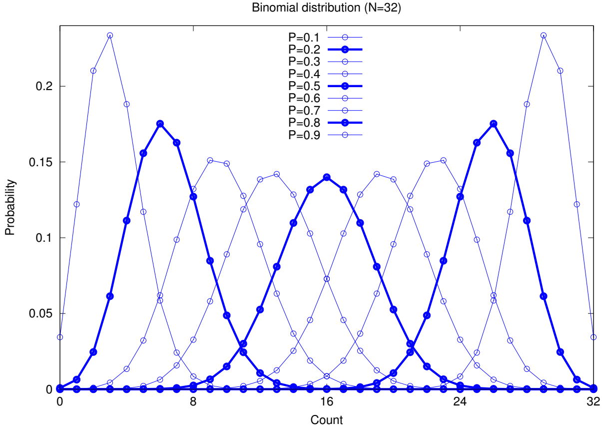

Figure: Stochastic resonance integration PMF.

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Symbol coding

- We are using symbols to transmit data. Related to:
  - Direct-Sequence Spread Spectrum (DSSS)
  - Direct-Sequence Code Division Multiple Access (DS-CDMA)
- We are using pulses (one per chip) instead of continuous waves.
- Chips are BPSK coded.

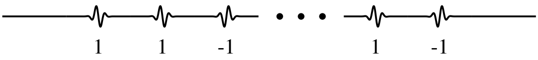

Figure: A symbol.

Symbol coding (2)

- Different symbols are different channels (Code Division Multiple Access (CDMA))
- Using low-interference (low cross-correlation) symbol codes (m-sequence, Barker, Walsh Hadamard, Gold, Kasami, WBE, GAWBE, “selected random”)

Example system parameters.

Example system parameters for our system:

- Pulse center frequency $f_c = 1$ GHz, any pulse shape
- $t_{\text{chip}} = 10$ ns
- Chips per symbol $Ns = 32$
- Pause to prevent Inter Symbol Interference (ISI). Symbol period: $t_{\text{symbol}} = 1$ μs $\Rightarrow$ Symbol rate: 1 MS/s

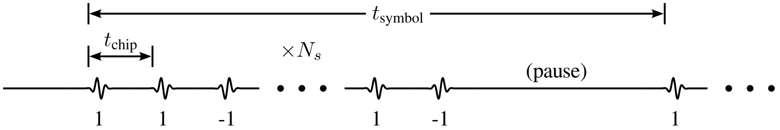

Figure: A symbol.

Transmitter and channel model signal flow.

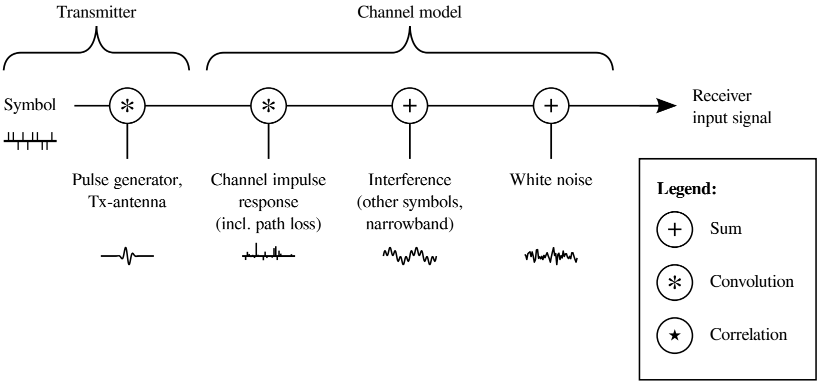

Figure: Transmitter and channel model signal flow.

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Simple ideal analog receiver signal flow.

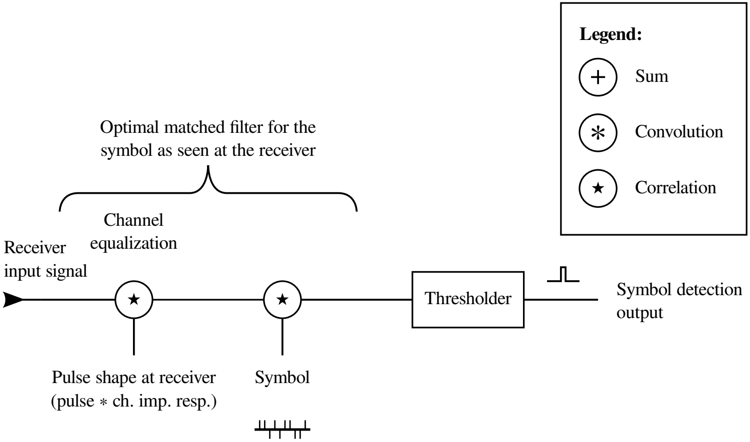

Figure: Simple ideal analog receiver signal flow.

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Stochastic resonance receiver signal flow.

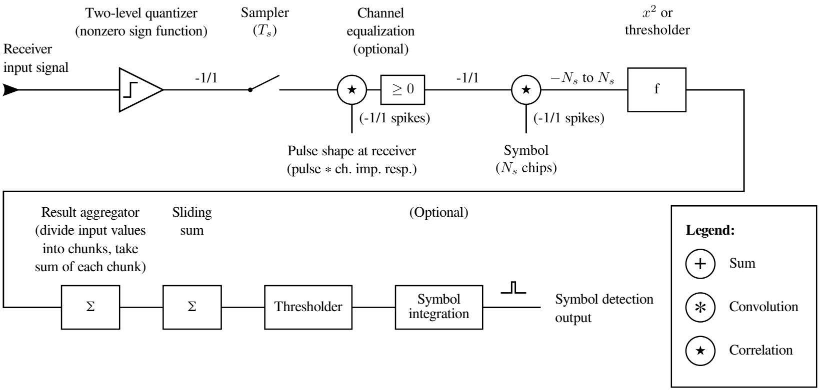

Figure: Stochastic resonance receiver signal flow.

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System overview

- Basically a RAKE receiver
- Parallelized structure to handle the high-speed computation (cross-correlation at multiple gigahertz)

Top level.

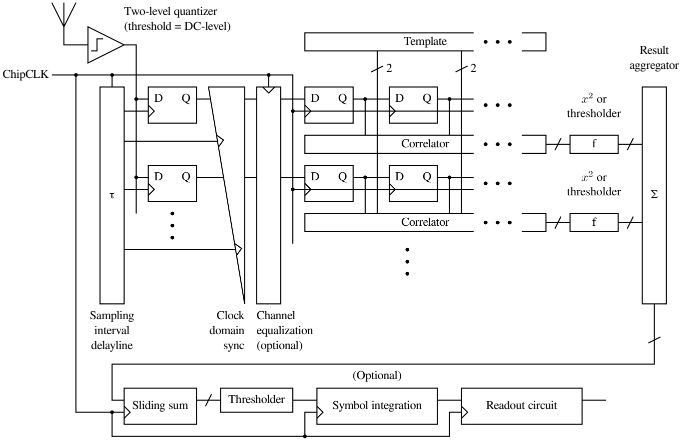

Figure: Top level.

Example system parameters.

Example system parameters for the chip:

- Pulse center frequency $f_c = 1$ GHz, any pulse shape $\Rightarrow$ $f_s \approx 4$ GHz (sampling-delayline)
- $t_{\text{chip}} = 10$ ns $\Rightarrow$ approx. 40 RAKE fingers
- Chips per symbol $Ns = 32 \Rightarrow$ RAKE finger length $= 32$

Sampling interval delayline.

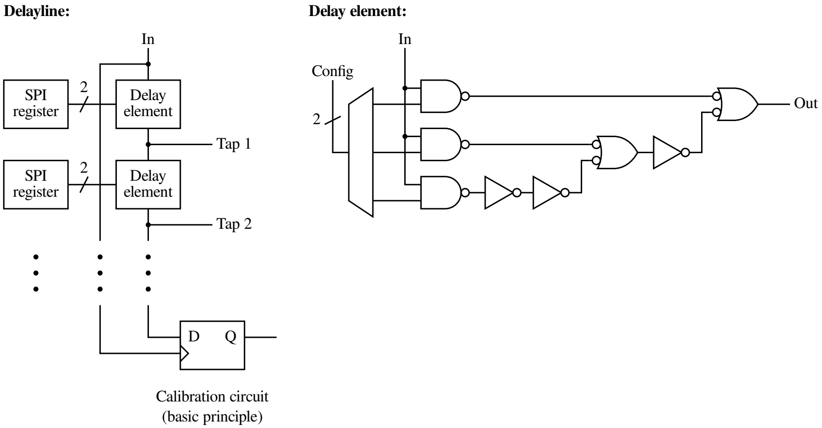

Figure: Sampling interval delayline.

Clock domain sync.

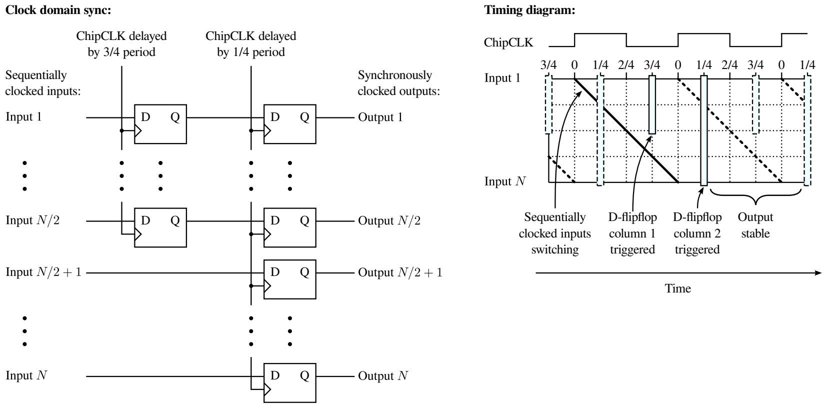

Figure: Clock domain sync.

Channel equalizer.

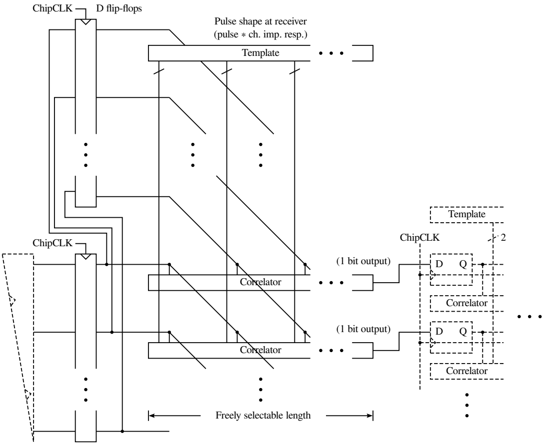

Figure: Channel equalizer.

Channel equalizer correlator.

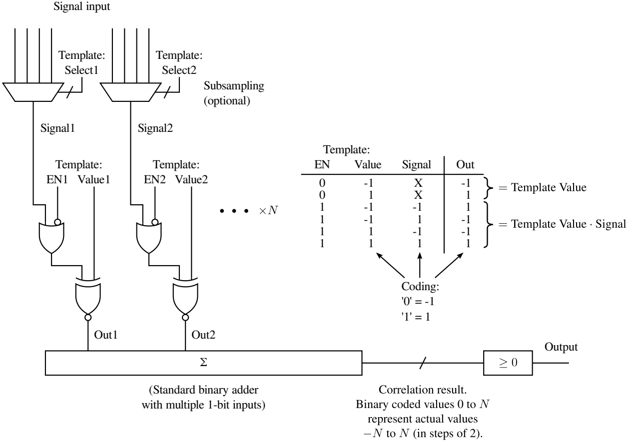

Figure: Channel equalizer correlator.

Main correlator.

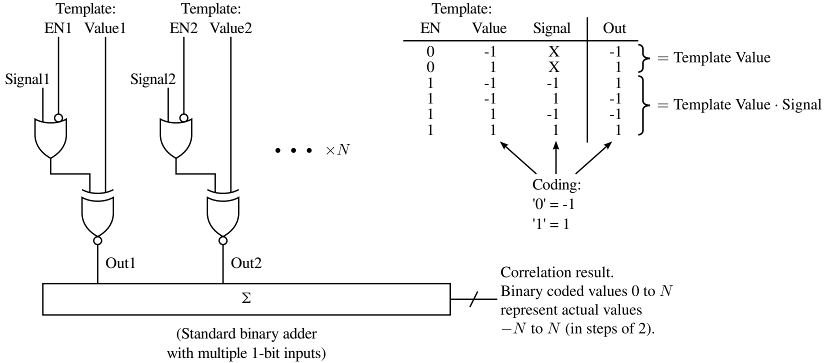

Figure: Main correlator.

Correlation value transform function f.

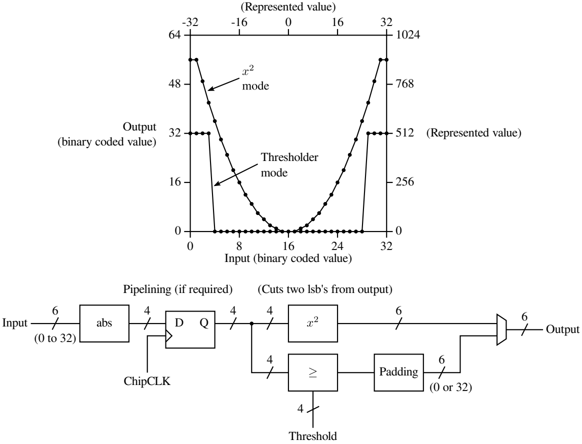

Figure: Correlation value transform function f.

Absolute value function.

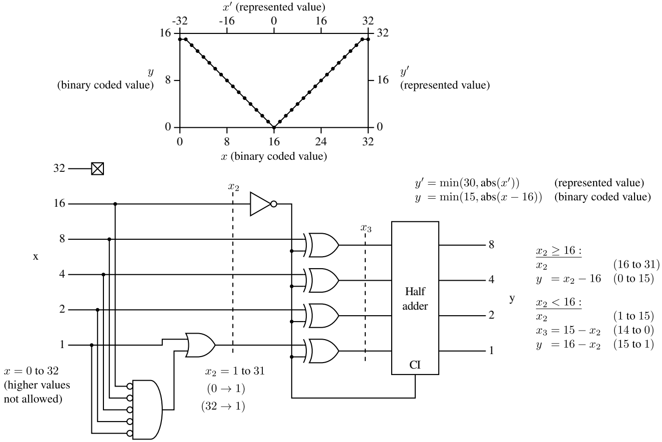

Figure: Absolute value function.

Squaring function.

```
% Exact:
y1   = x1;
y2   = 0;
y4   = x2 & !x1;
y8   = x1 & xor(x4, x2);
y16  = (x1 & xor(x8, x4)) | (x4 & !x2 & !x1);
y32  = (x2 & xor(x8, x4)) | (x8 &  x4 &  x1);
y64  = x8 & !(x4 & !x2);
y128 = x8 & x4;
% Implementation (4 not, 6 nand, 9 nor):
% TSMC 90nm TCBN90GHP-lib cellwidths:
%   not: 0.28um*3, nand: 0.28um*4, nor: 0.28um*4.
% Total: 0.28um * (3*4 + 4*6 + 4*9) = 20.160um.

% Truncate to 6 bit output, which gives max 2% error for x > 3:
y1 = 0;
y2 = 0;
scale = 1.02;
```

Figure: Squaring function.